

1

Title			
BLOCK DIAGRAM			
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ICH8M Functional Strap Definitions

ICH8-M EDS 21762 2.0V1 page 16

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments.

ICH8M IDE Integrated Series
Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

PCI Routing

page 17

	IDSEL	INT	REQ	GNT
TI7412	AD22	G:CARDBUS B:1394 F:Flash Media G:SD Host	0	0

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB	
Pair	Device
0	USB1
1	USB4
2	USB2
3	FT
4	USB3
5	BLUETOOTH
6	NC
7	MINICARD
8	WEBCAM
9	NEW1

ICH8M Integrated Pull-up
and Pull-down Resistors

ICH8-M EDS 21762 2.0V1

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

History

Crestline Strapping Signals and
Configuration

Crestline EDS 20954 1.0
page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG[8:6]	Reserved	
	Low Power PCI Express	0 = Normal mode 1 = Low Power mode (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL _DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading
edge of the Crestline GMCH PWORK in signal.

UMA

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6 H_A#(35..3) <<>> H_A#(35..3)

6 H_ADSTB#0 <<>> H_ADSTB#0

6 H_REQ#(4..0) <<>> H_REQ#(4..0)

6 H_ADSTB#1 <<>> H_ADSTB#1

16 H_A20M# <<>> H_A20M#

16 H_FERR# <<>> H_FERR#

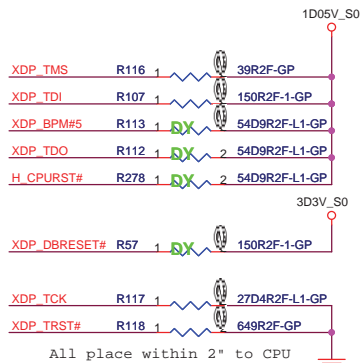
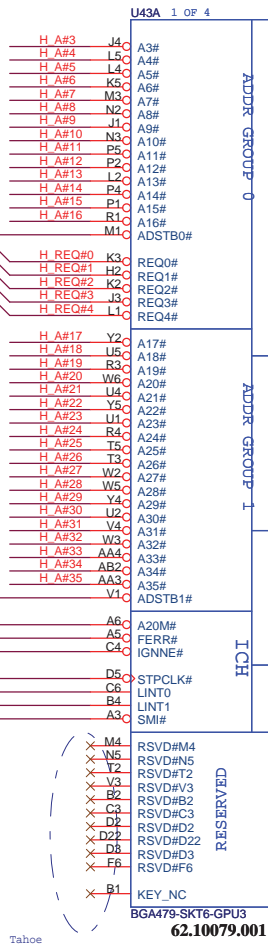
16 H_IGNNE# <<>> H_IGNNE#

16 H_STPCLK# <<>> H_STPCLK#

16 H_INTR <<>> H_INTR

16 H_NMI <<>> H_NMI

16 H_SMI# <<>> H_SMI#



Place testpoint on H_IERR# with a GND 0.1" away

Layout Note:
"CPU_GTLREF0"
0.5" max length.

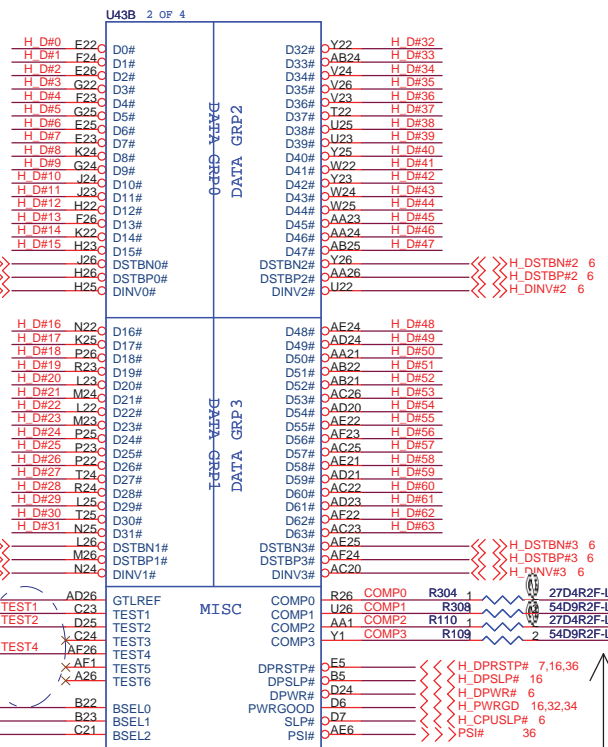
Net "TEST4" as short as possible,
make sure "TEST4" routing is
reference to GND and away from
noisy signals

H_DINV#(3..0) <<>> H_DINV#(3..0) 6

H_DSTBN#(3..0) <<>> H_DSTBN#(3..0) 6

H_DSTBP#(3..0) <<>> H_DSTBP#(3..0) 6

H_D#(63..0) <<>> H_D#(63..0) 6



Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make
trace length shorter than 0.5"
Comp1, 3 connect with Zo=55 ohm, make
trace length shorter than 0.5"

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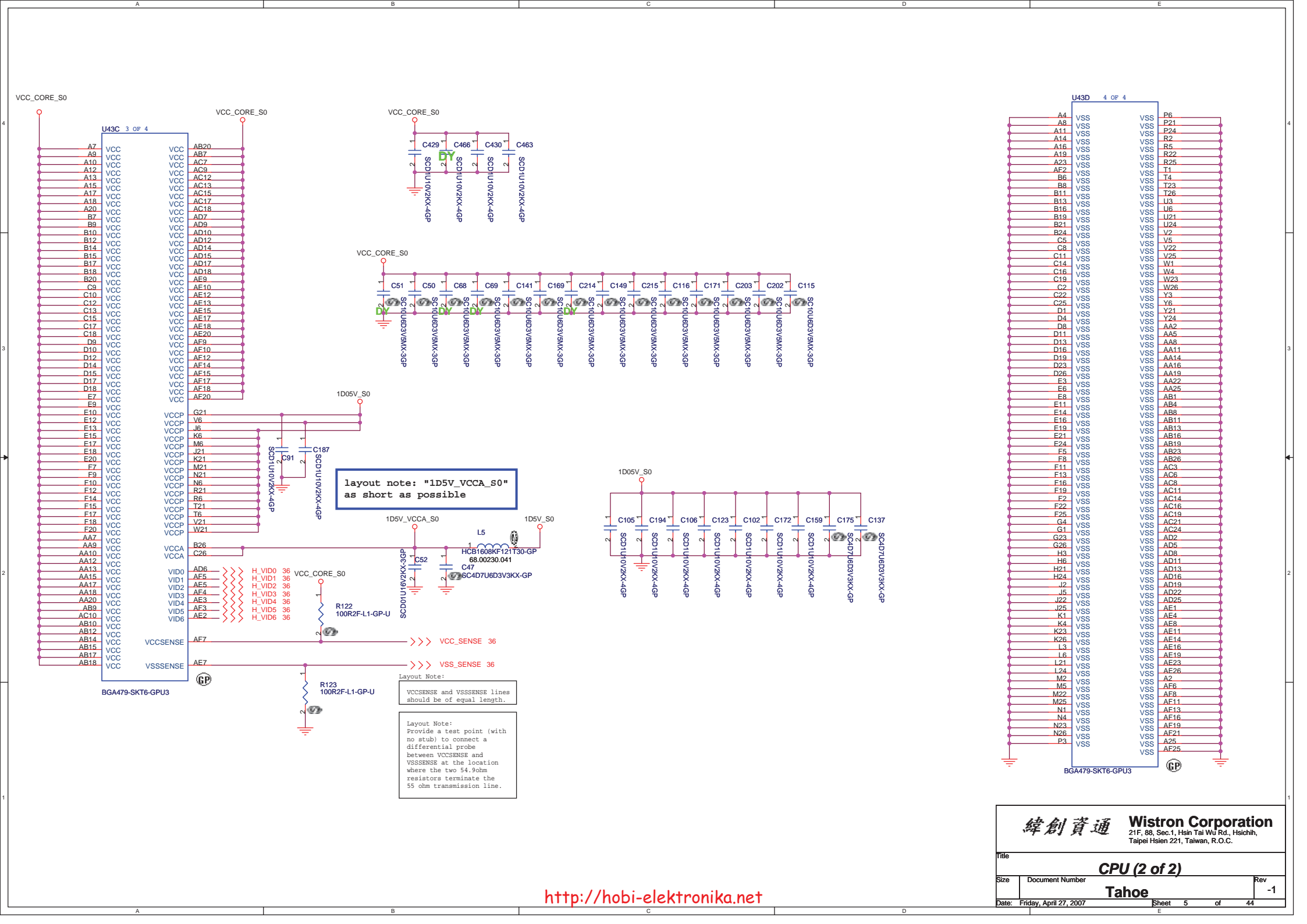
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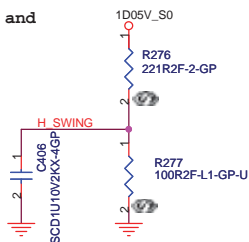
CPU (1 of 2)

Tahoe



H_SWING routing Trace width and Spacing use 10 / 20 mil

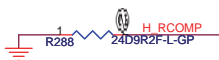
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_SCOMP and H_SCOMP# Resistors and Capacitors close MCH 500 mil (MAX)

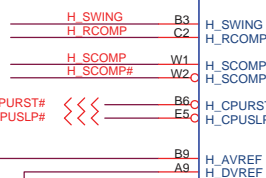
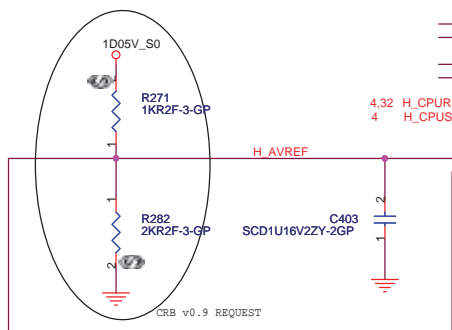


H_RCOMP routing Trace width and Spacing use 10 / 20 mil

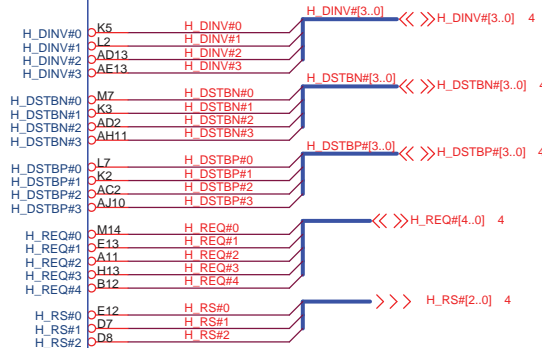
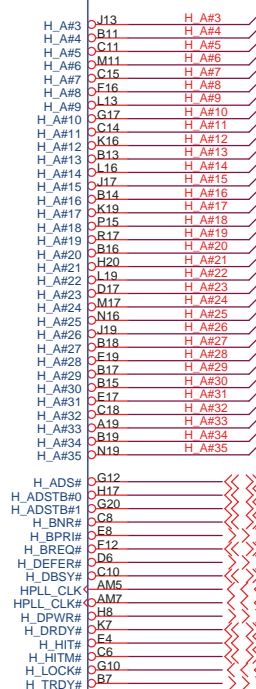
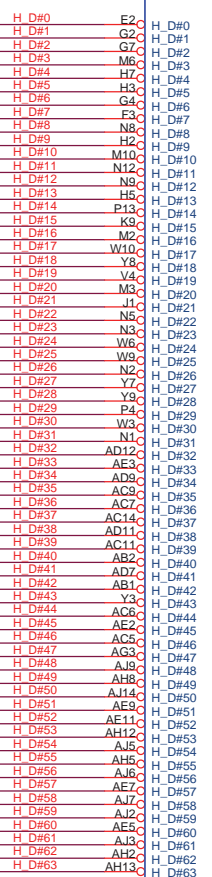


Place them near to the chip (< 0.5")

H_REF Decoupling Crestline close Crestline 100 mil



U42A 1 OF 10

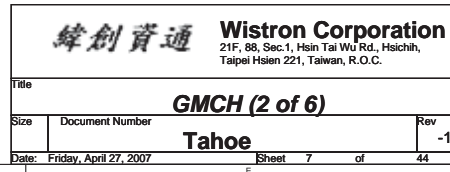


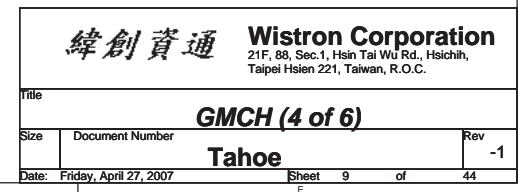
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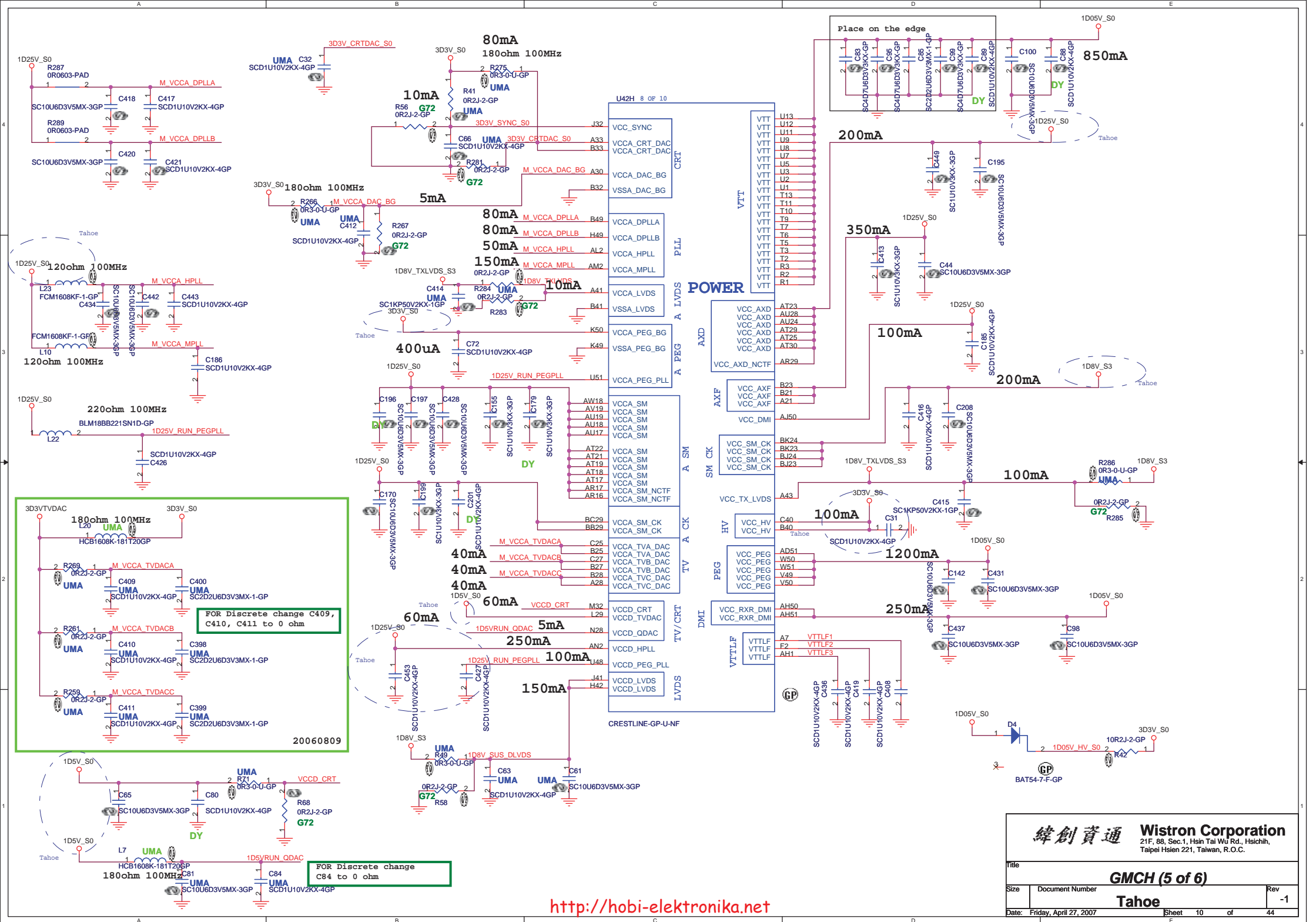
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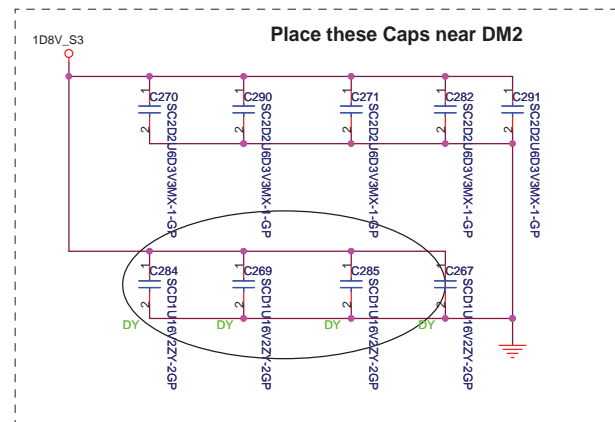
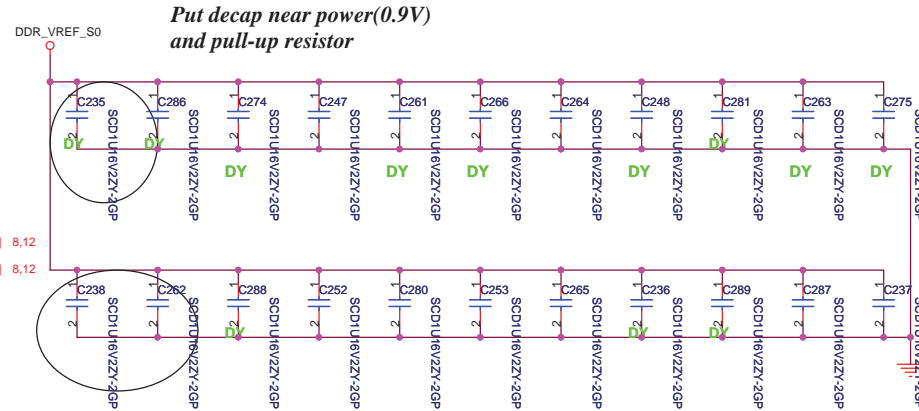
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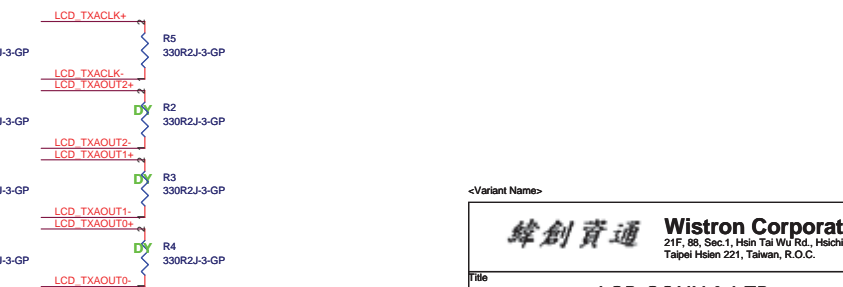
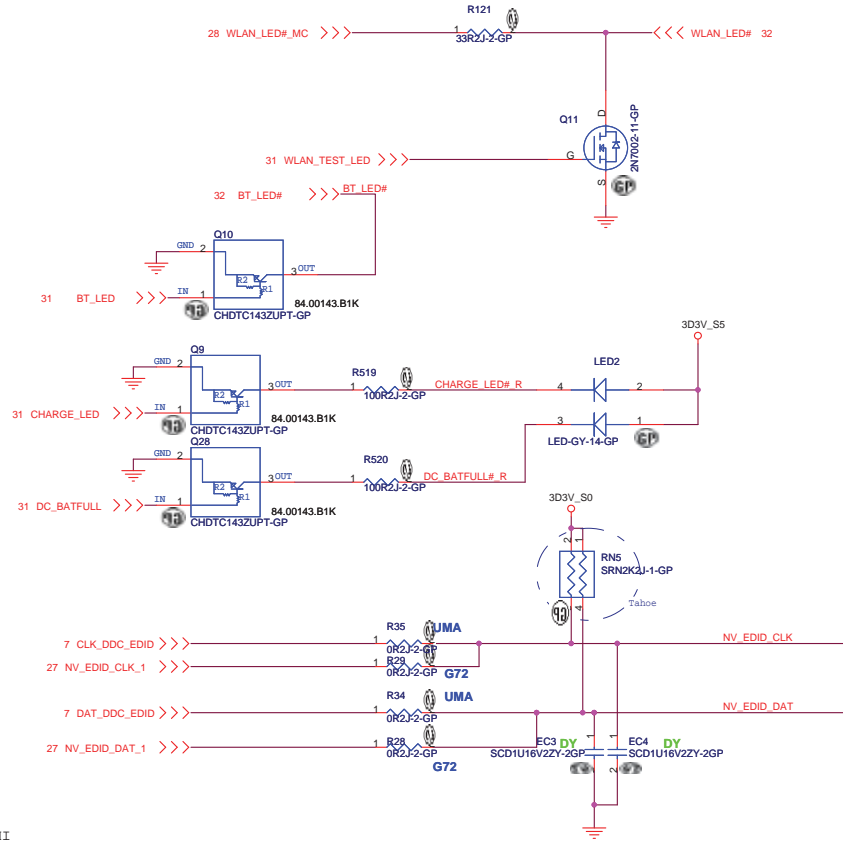
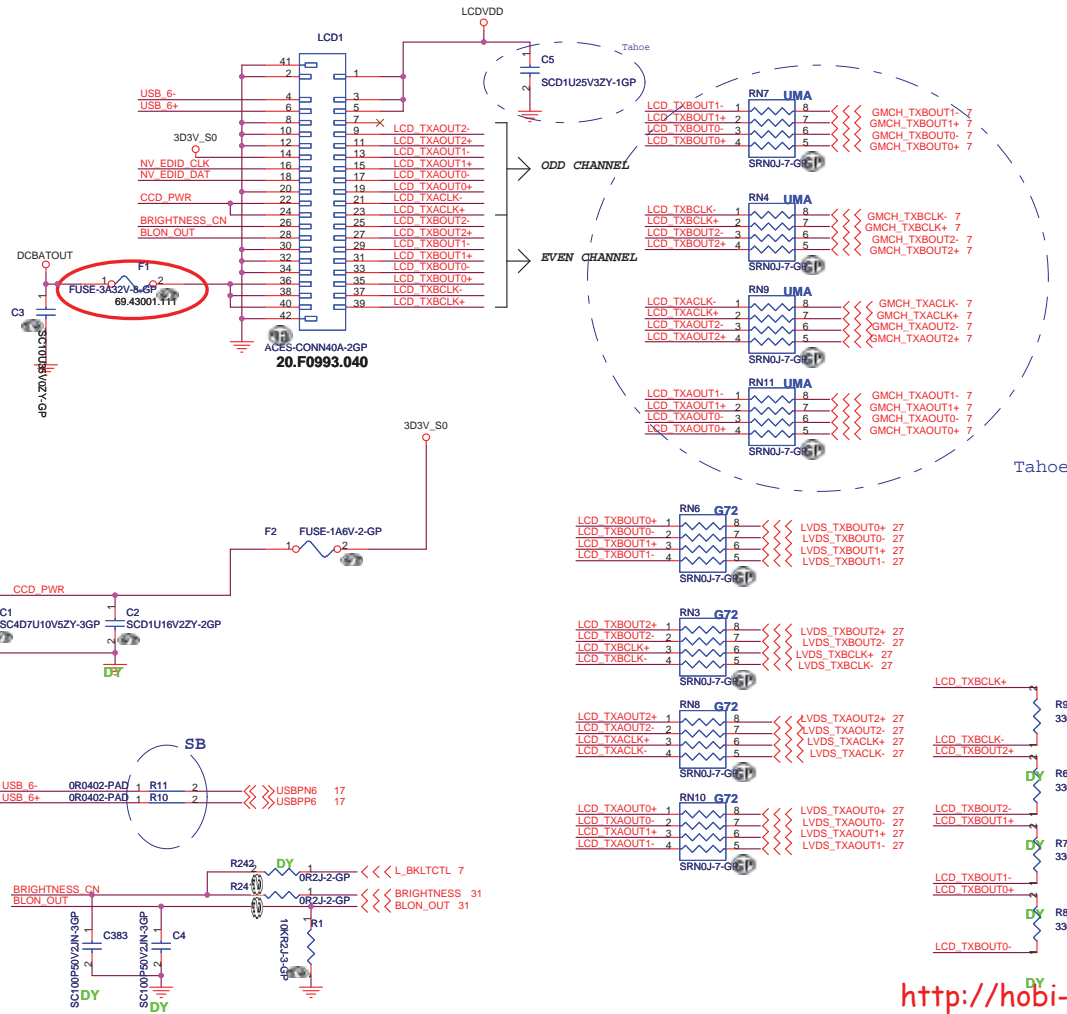
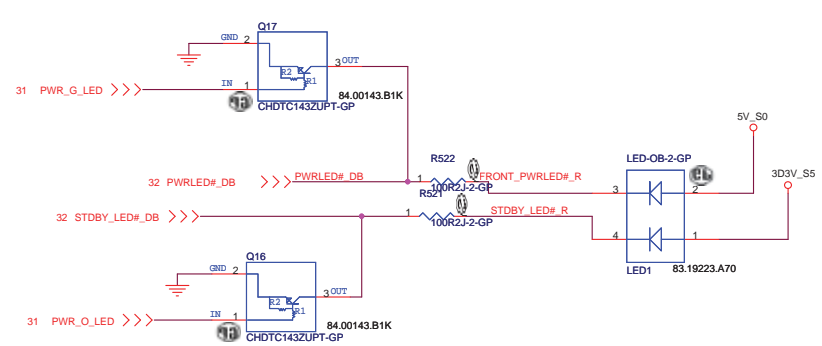
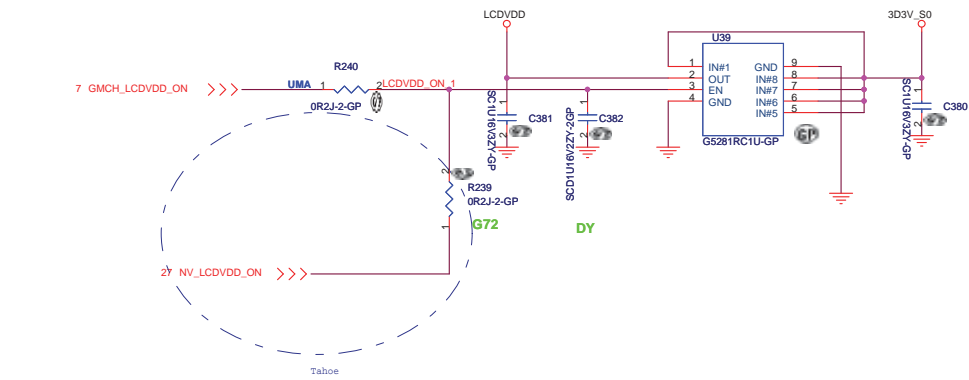




Decoupling Capacitor

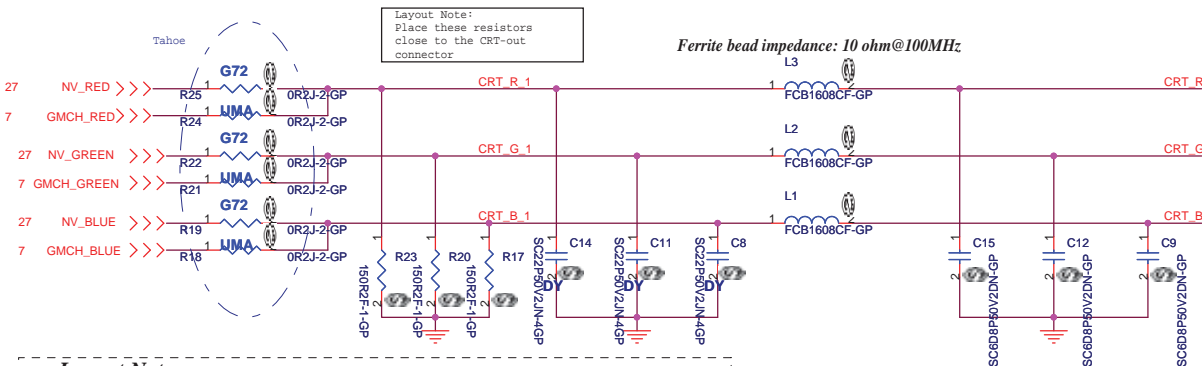


LCD/INVERTER CONN



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CRT I/F & CONNECTOR



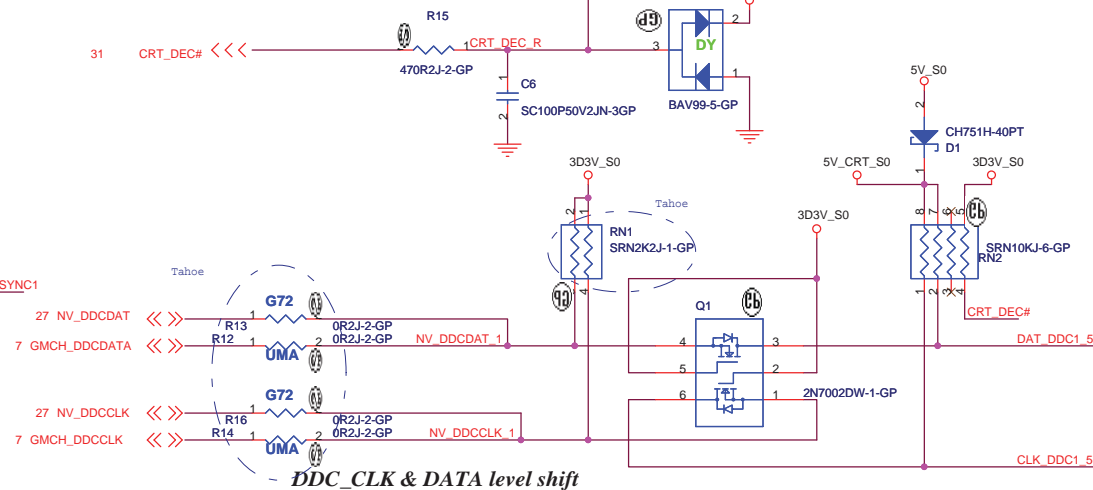
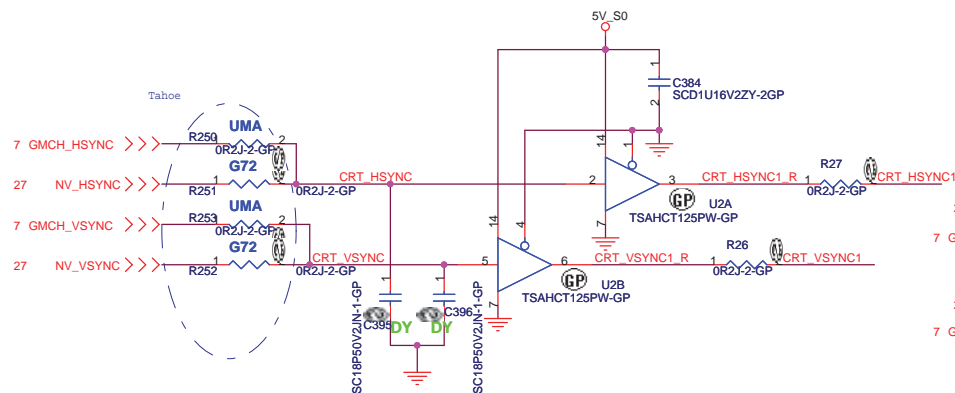
Layout Note:

* Must be a ground return path between this ground and the ground on the VGA connector.

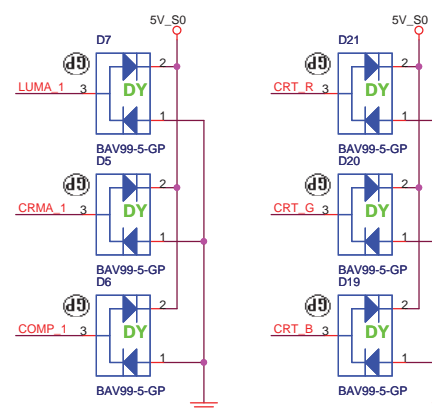
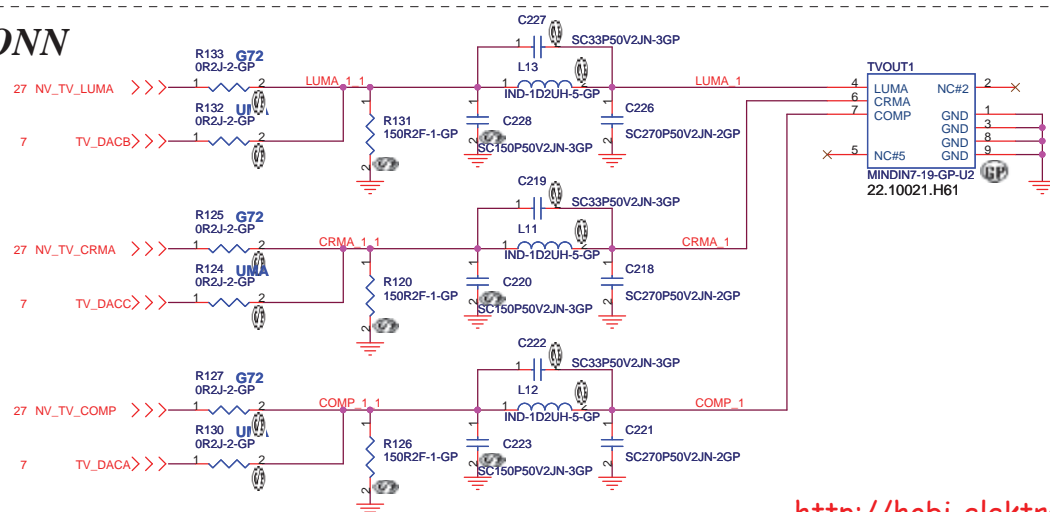
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

For DIS
C15---->78.15034.1FL
C12,C9---->78.18034.1FL

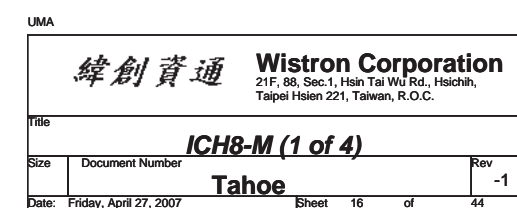
Hsync & Vsync level shift

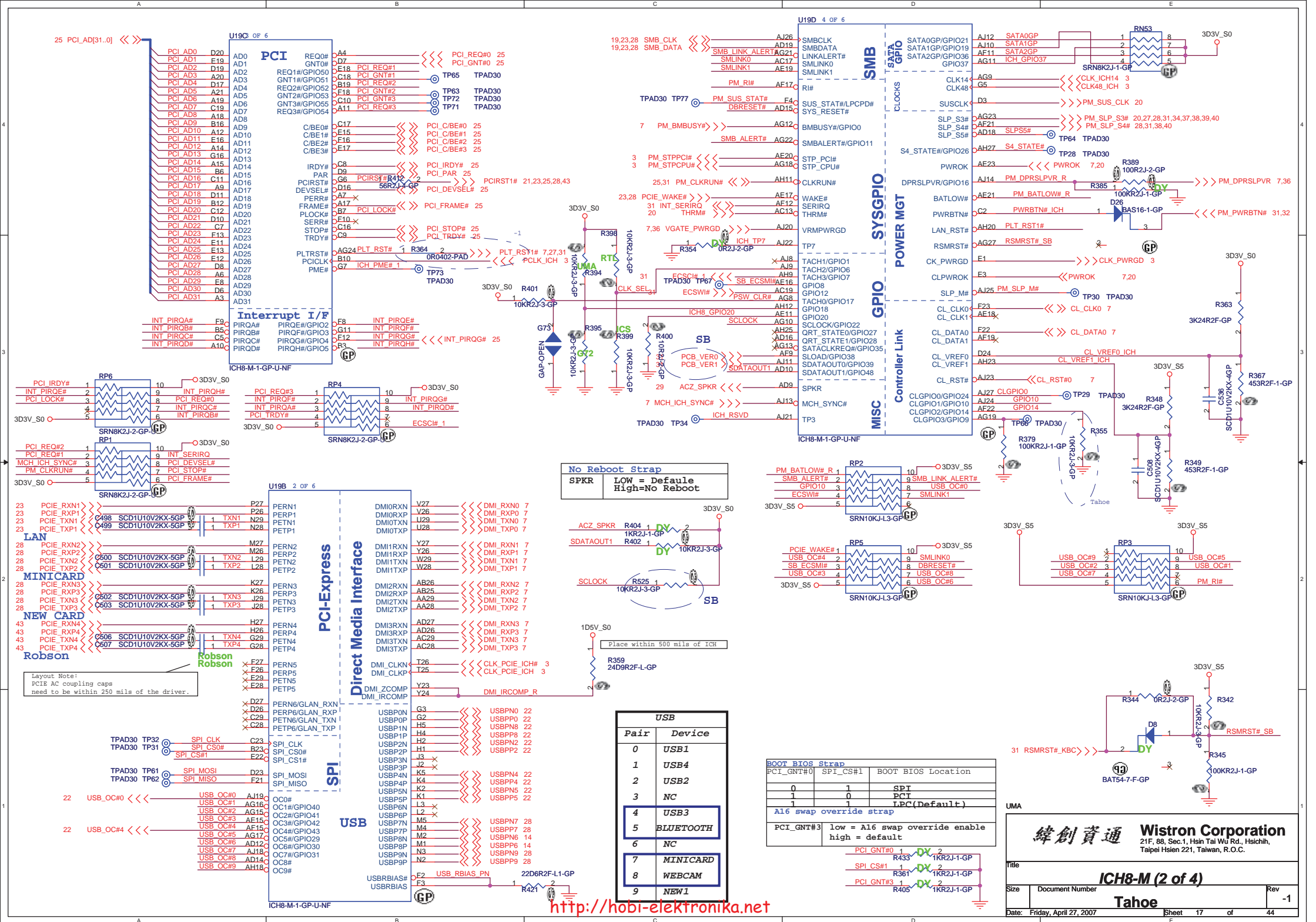


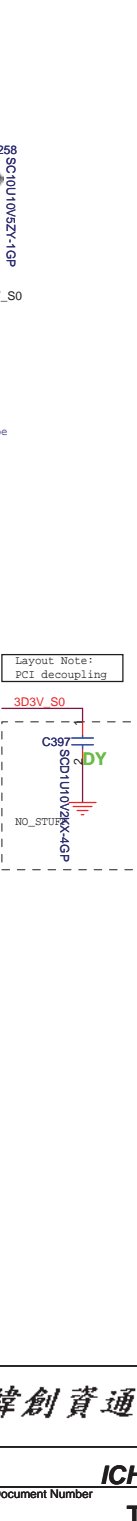
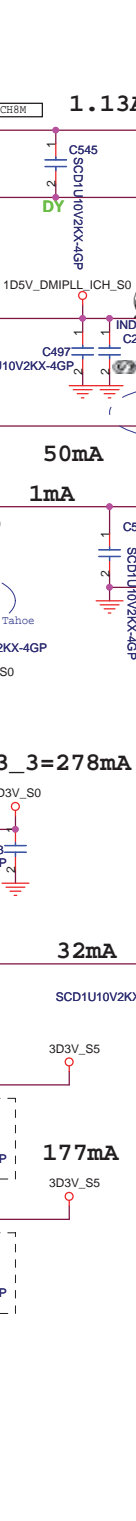
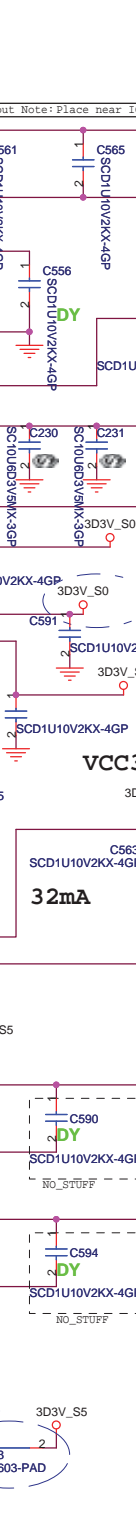
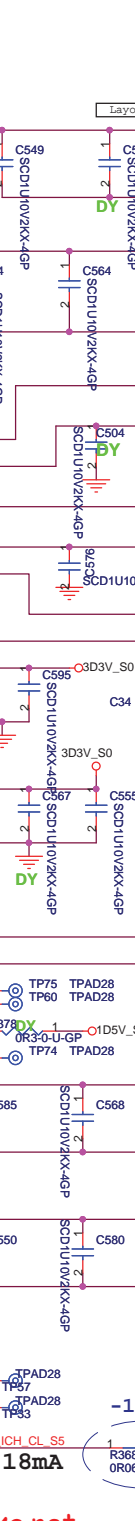
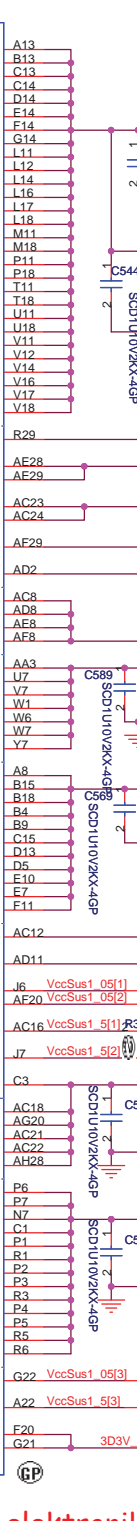
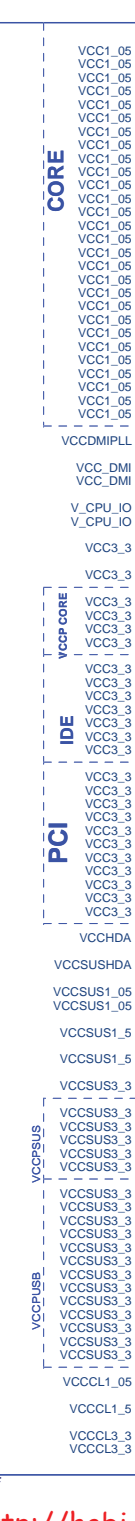
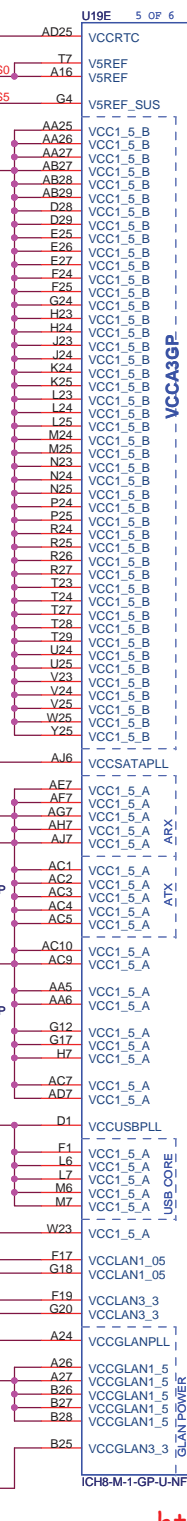
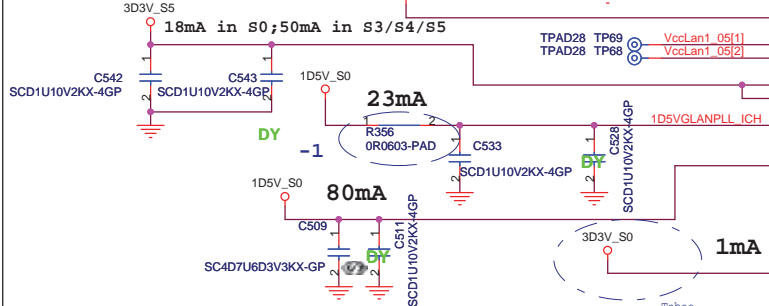
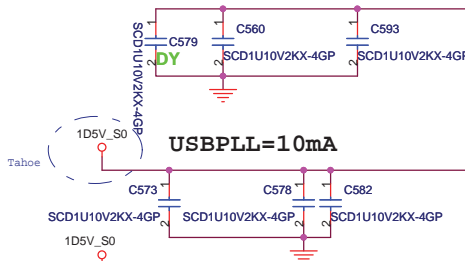
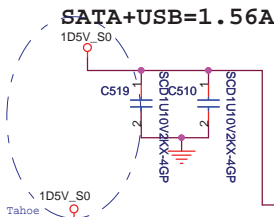
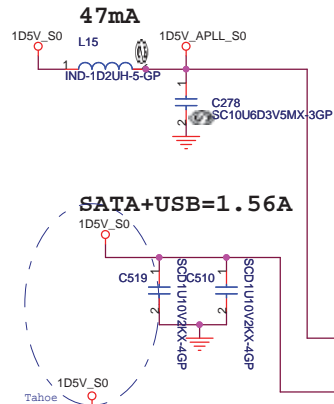
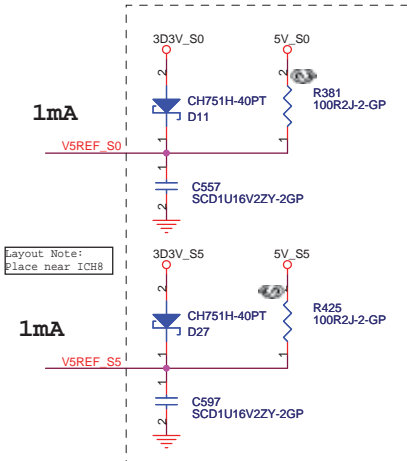
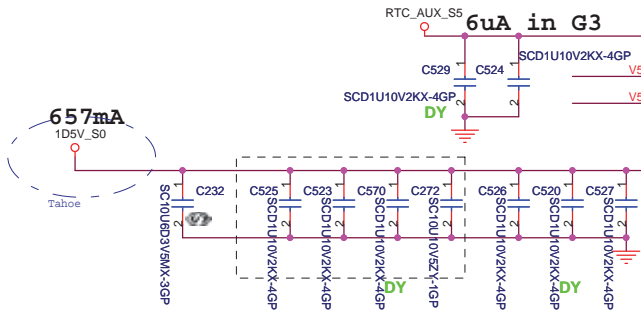
TV CONN

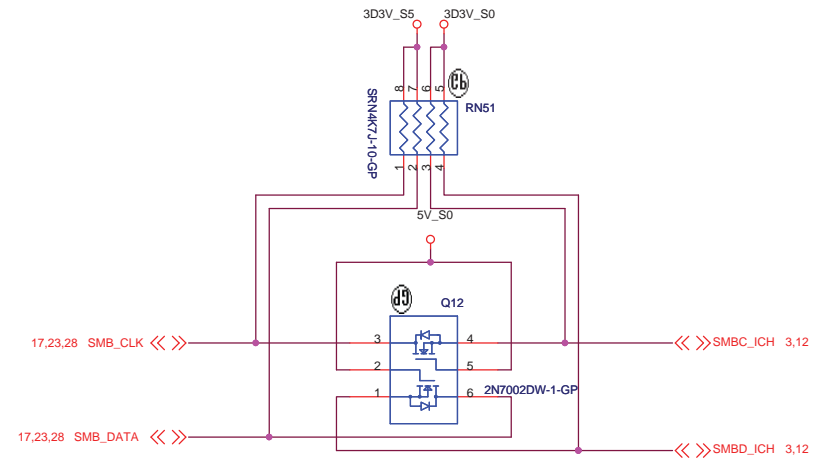
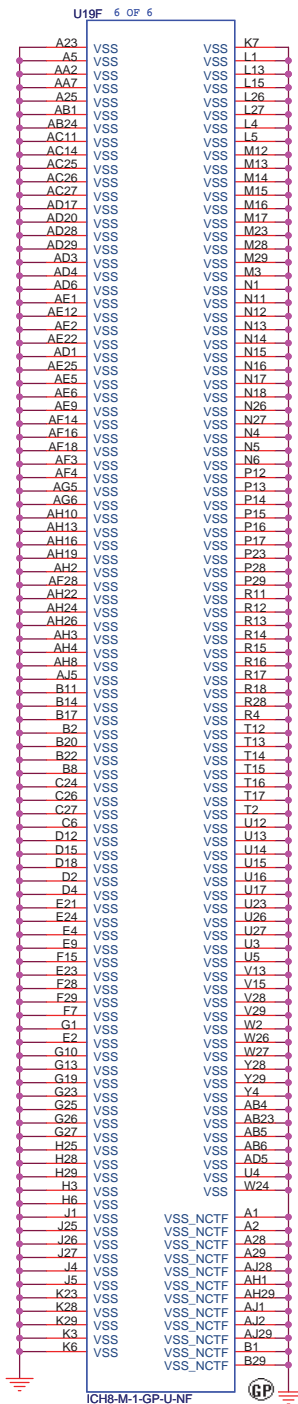


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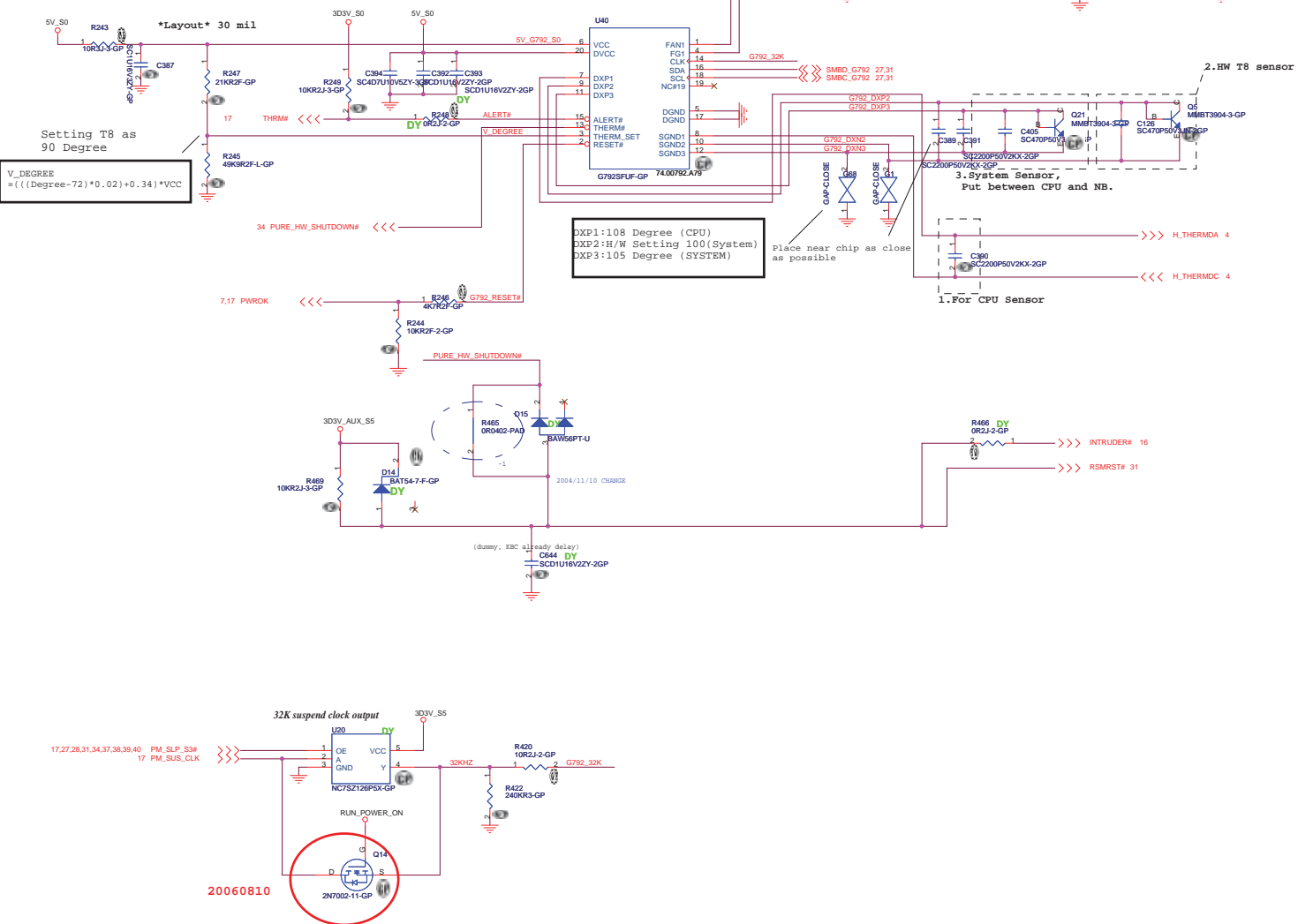




Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

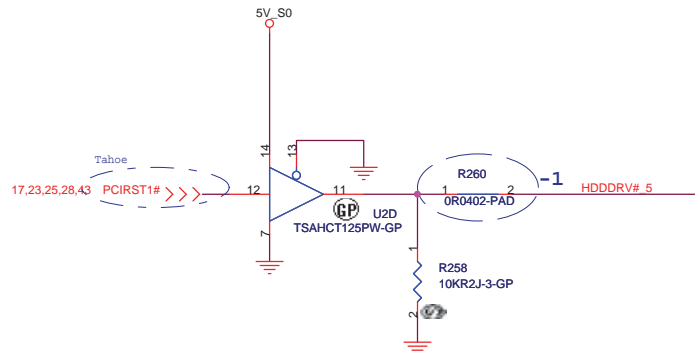
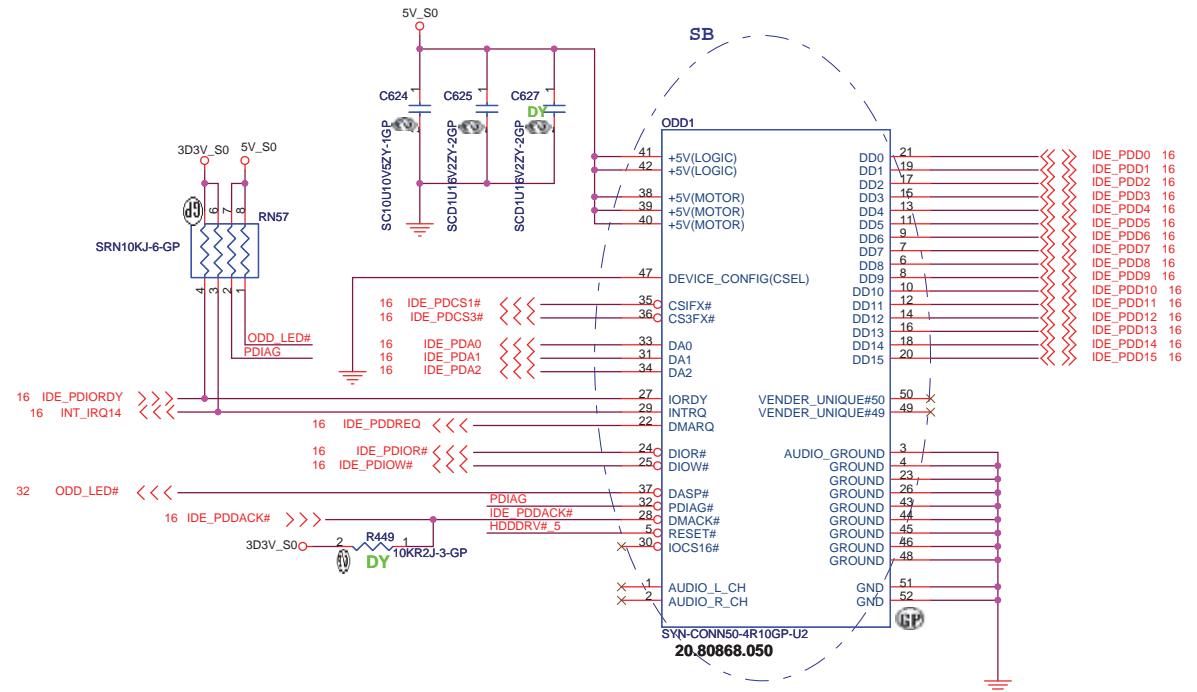
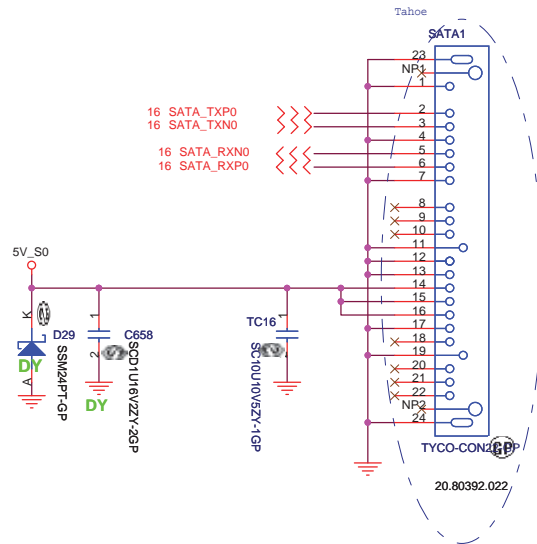
SMBUS

TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000



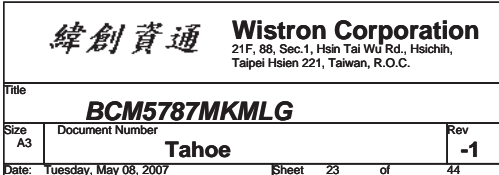
SATA HD Connector

ODD Connector



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bom1



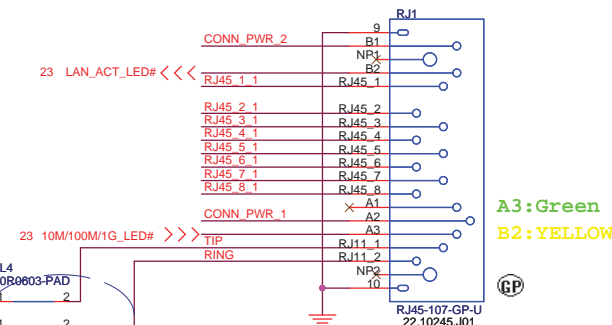
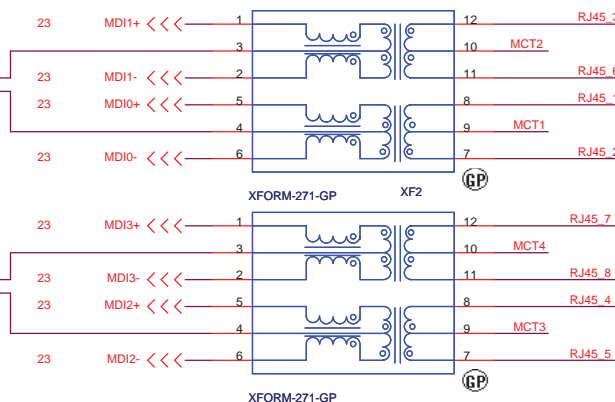
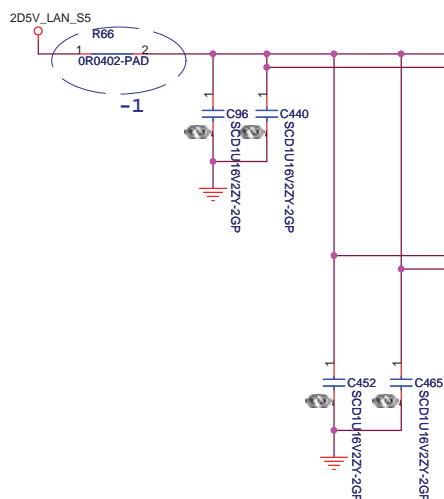
Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	

LAN Connector

-1 Test Point

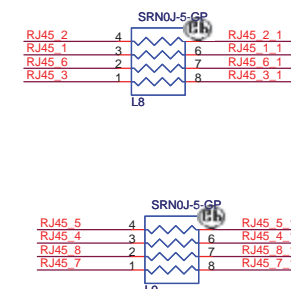


GIGA Lan Transformer



LAN Link: Green(A3), behavior is the same for 10/100/1000 bits
LAN Data: Yellow(B2), when LAN is transferring data.

For EMI

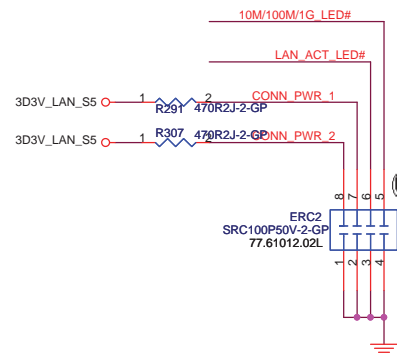
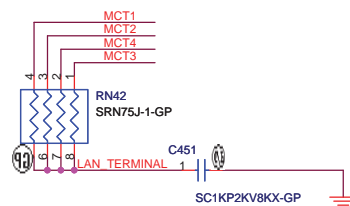


- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6



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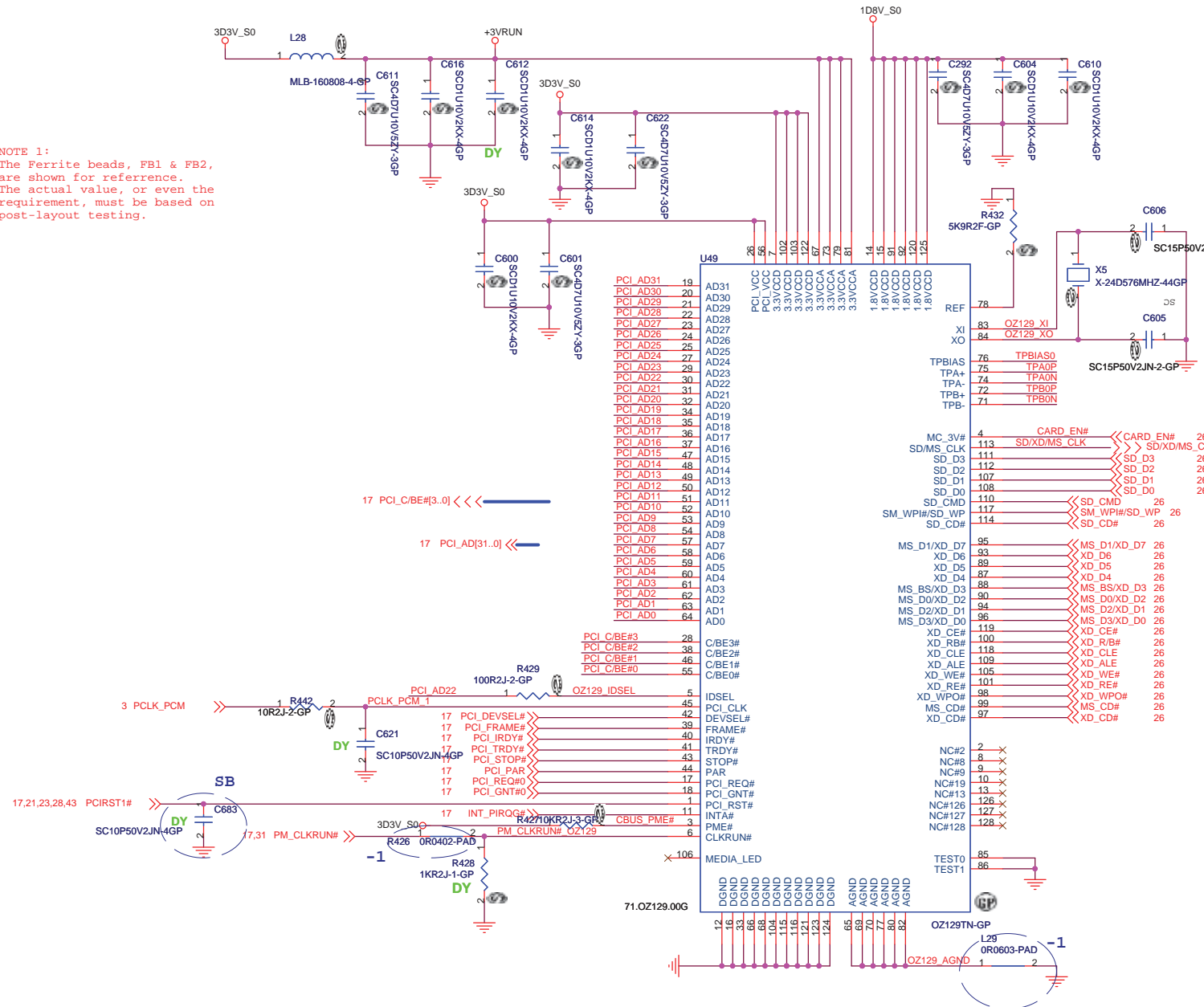
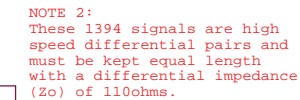
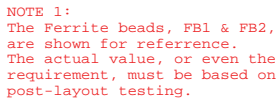
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緯創資通 Wistron Corporation
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Title: **LAN Connector**

Size A3 Document Number: **Tahoe** Rev: **-1**

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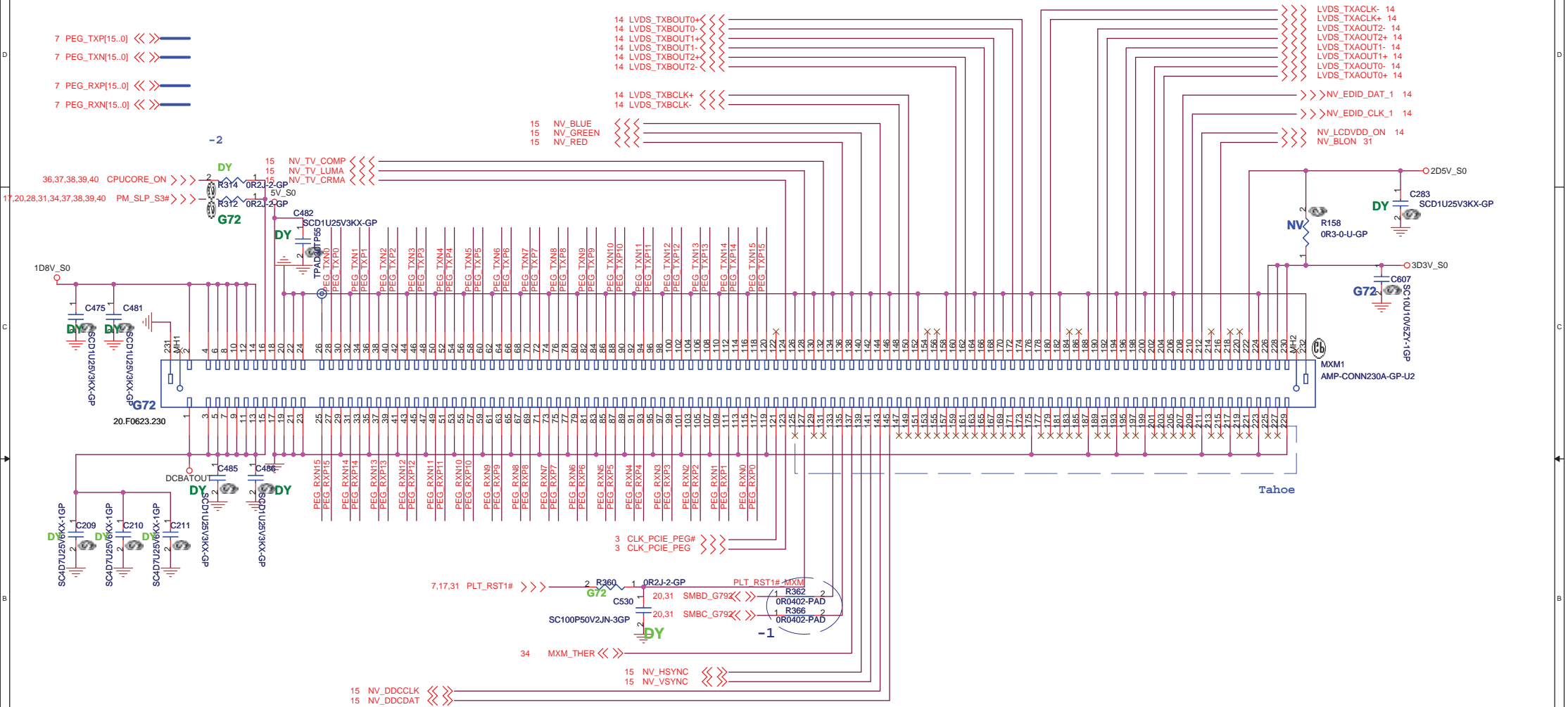


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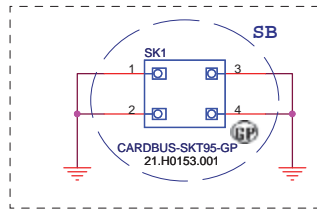

<Core Design>

Title			
Graphic MXM CONN			
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<http://hobi-elektronika.net>

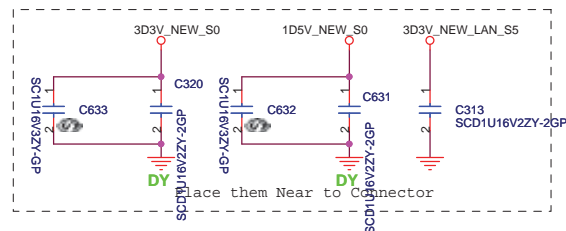
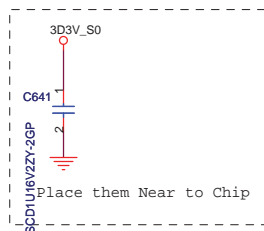
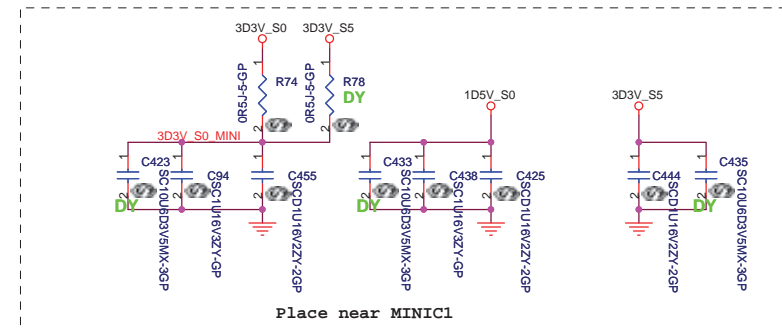
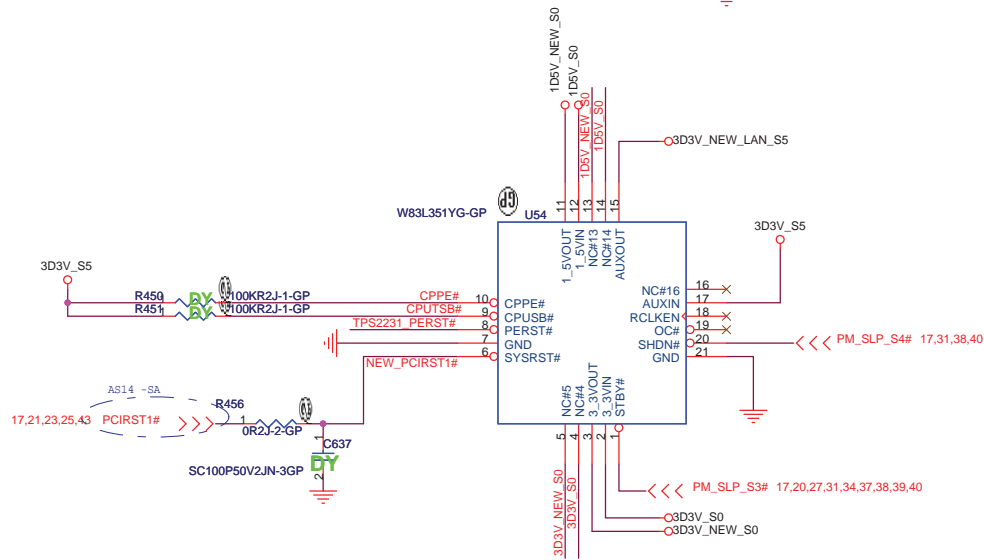
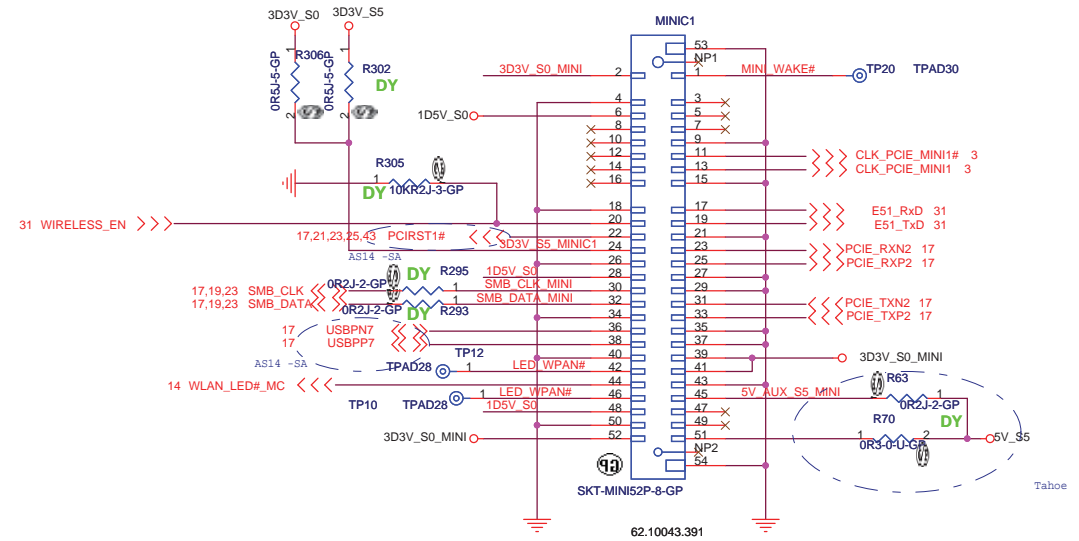


Mini Card Connector



NEWCARD Connector

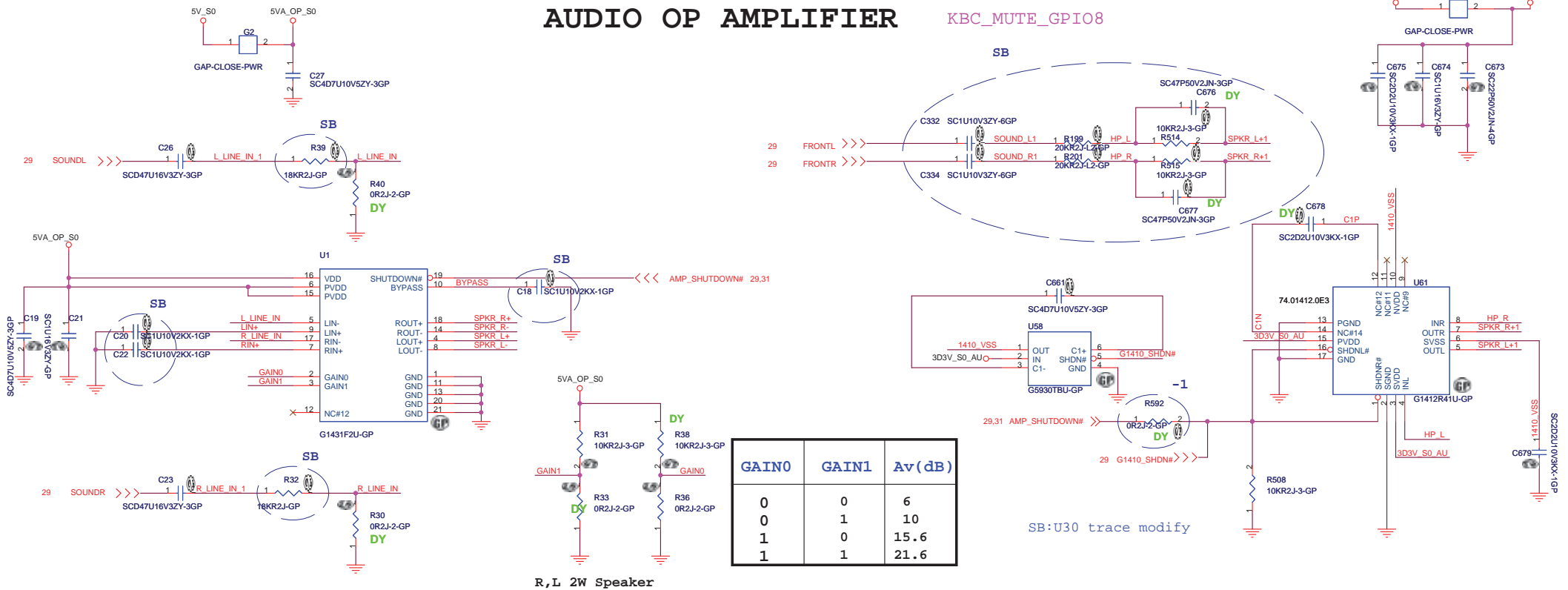
Reserve the symbol
for bottom side
connector





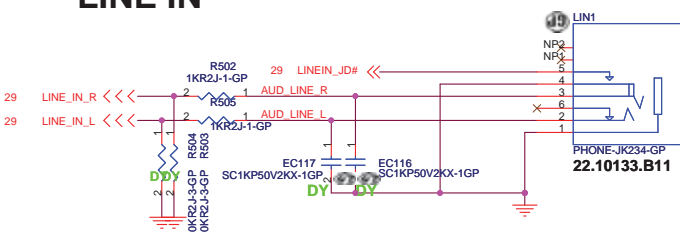
AUDIO OP AMPLIFIER

KBC_MUTE_GPIO8

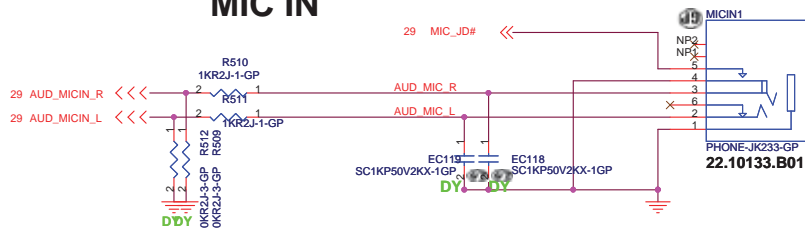


R,L 2W Speaker

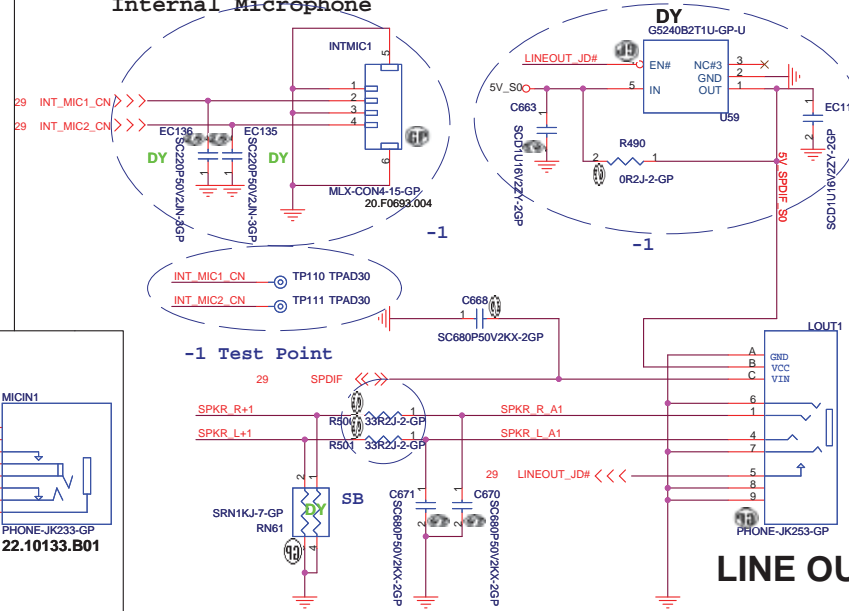
LINE IN



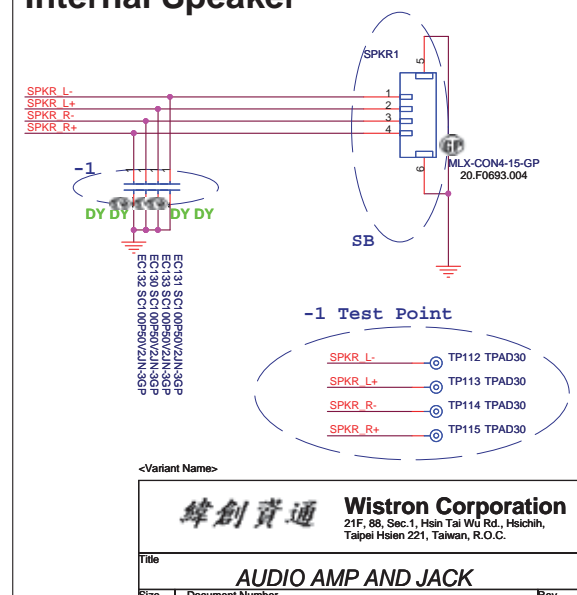
MIC IN



Internal Microphone



Internal Speaker



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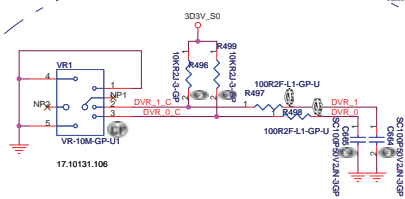
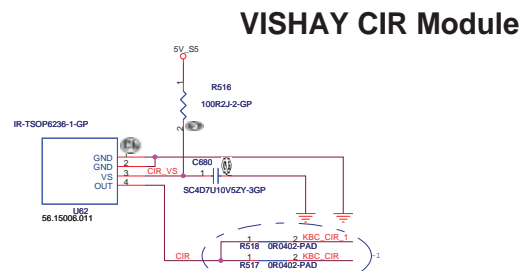
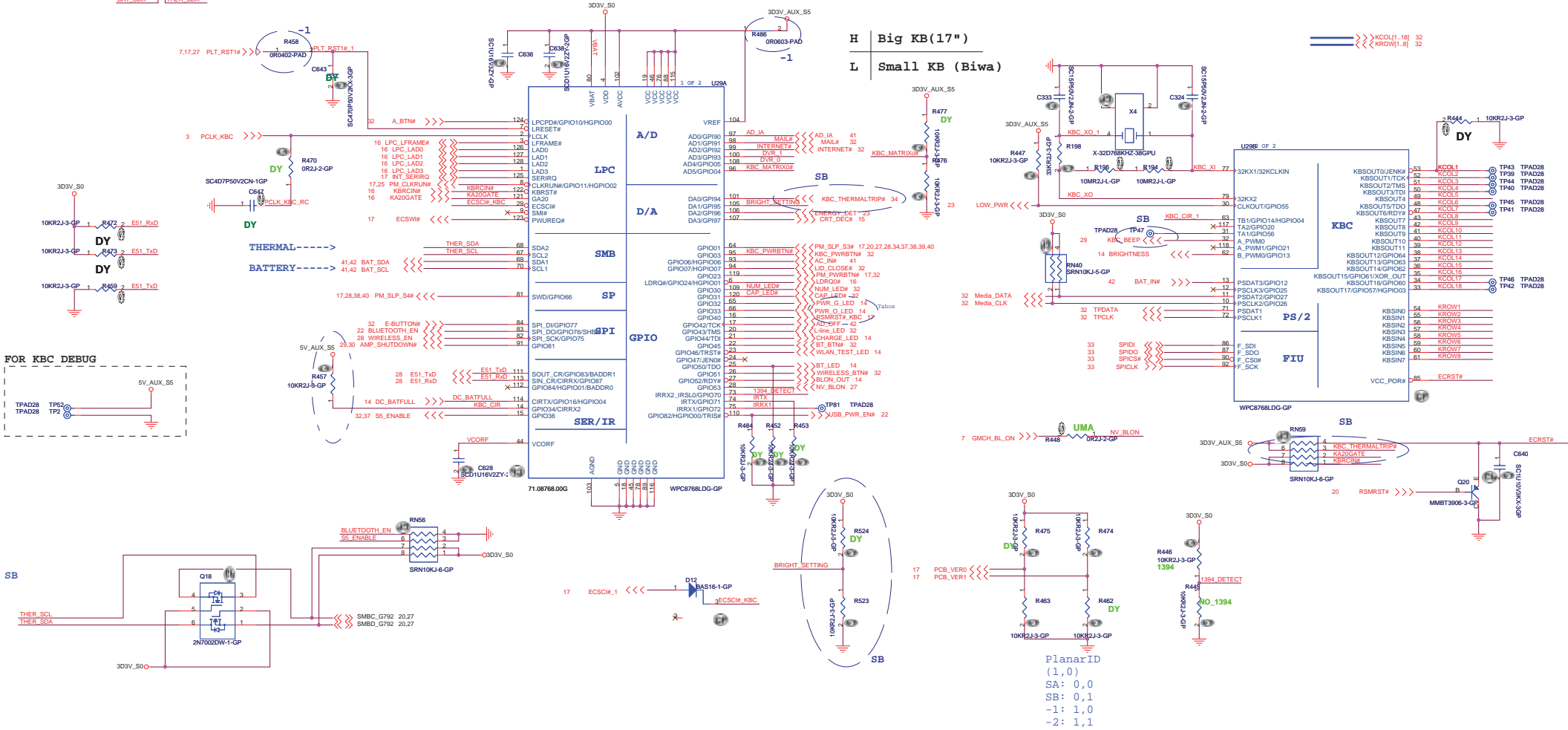
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緯創資通

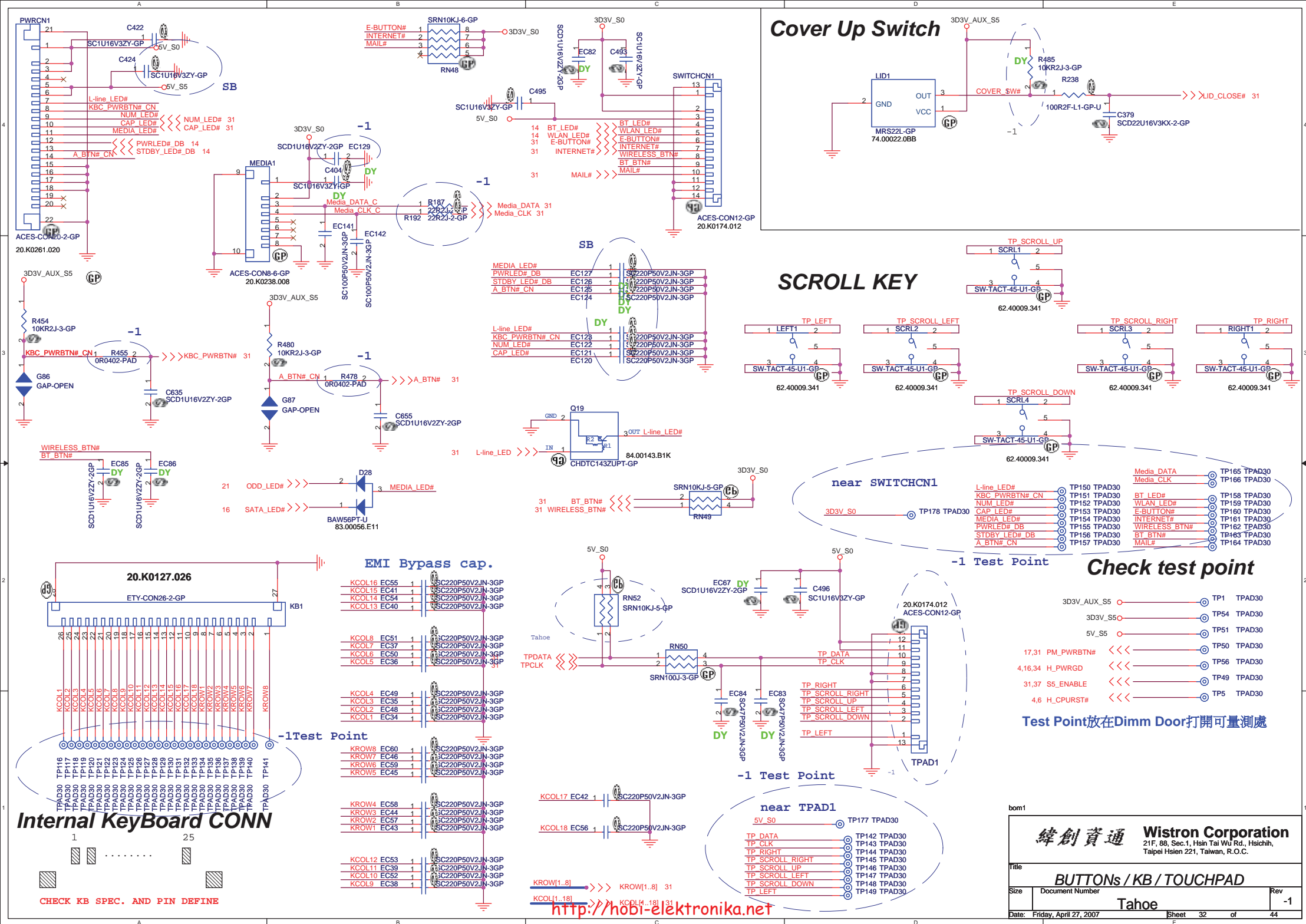
Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

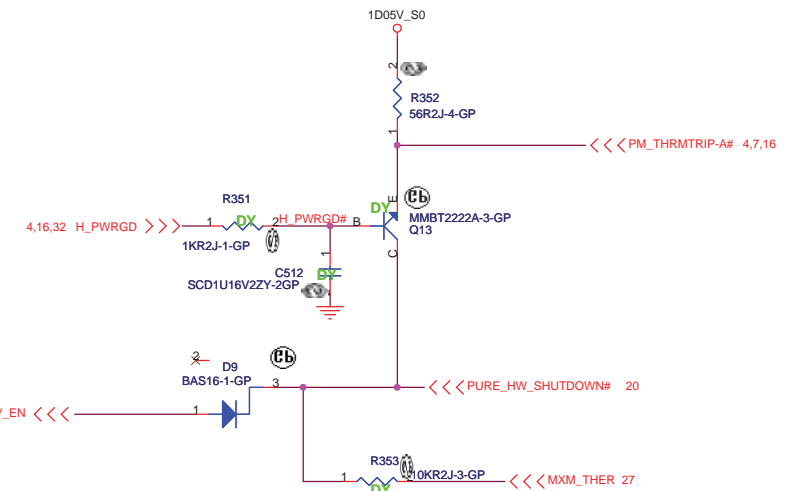
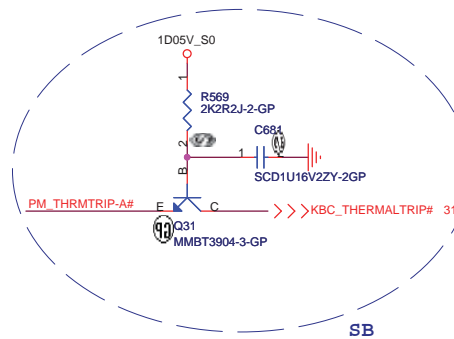
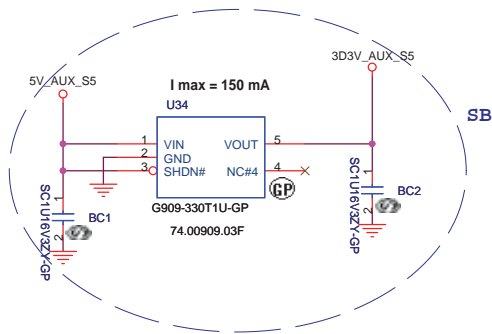
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AUDIO AMP AND JACK			
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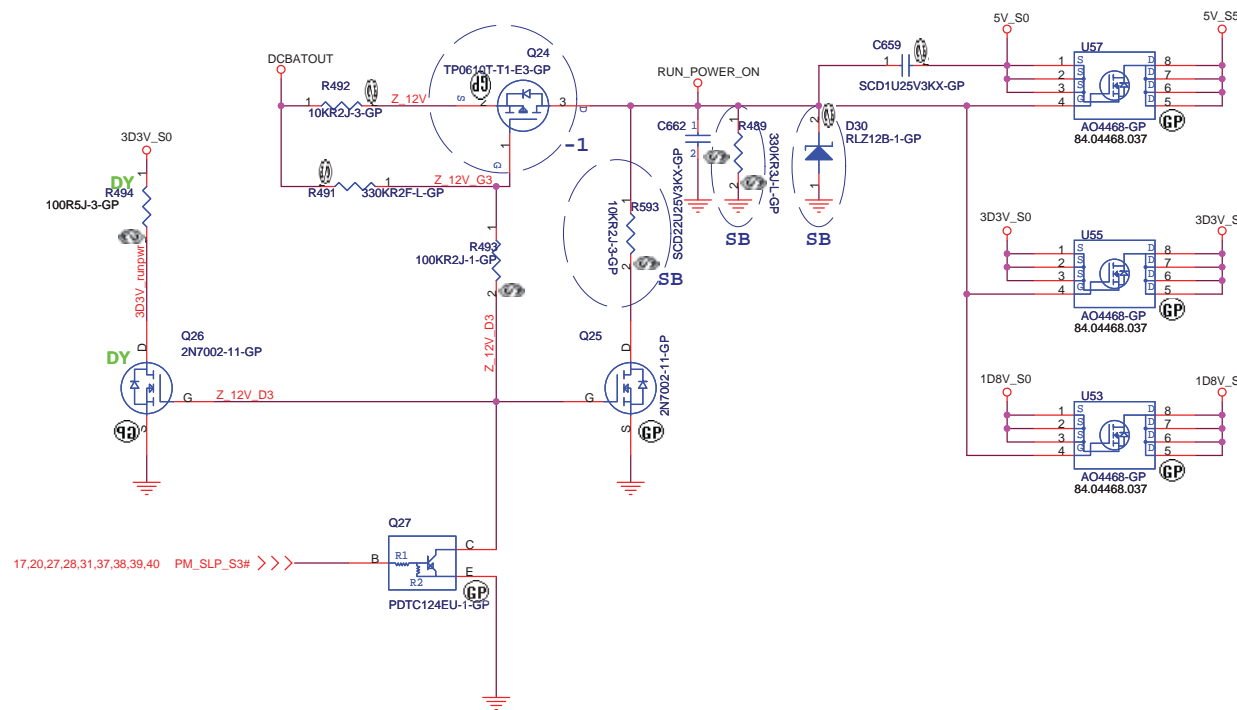
<http://hobi-elektronika.net>



Aux Power 3D3V_AUX_S5



Run Power

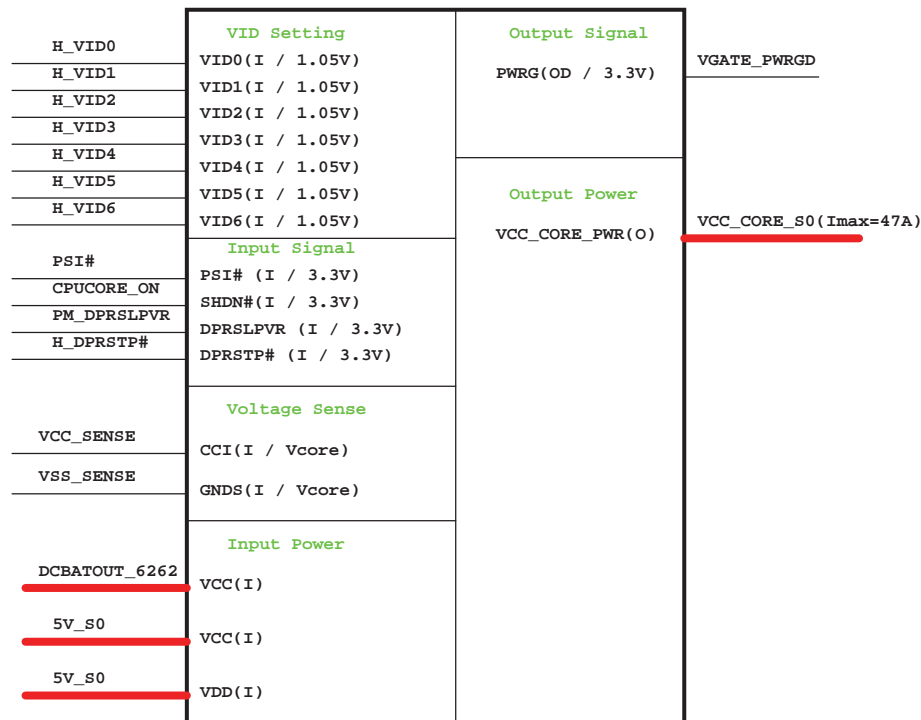


<http://hobi-elektronika.net>

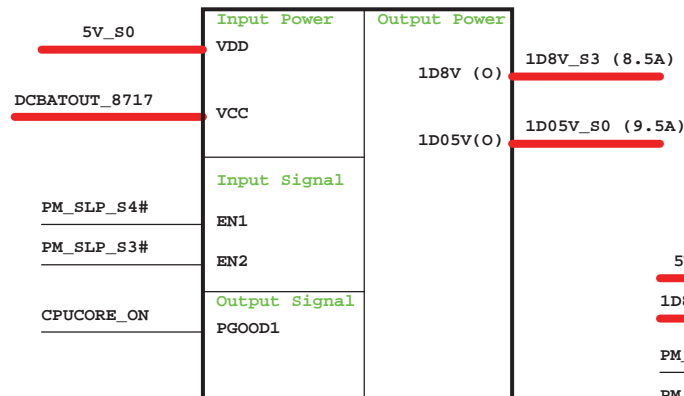
UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	RUN POWER and 3D3V_AUX_S5
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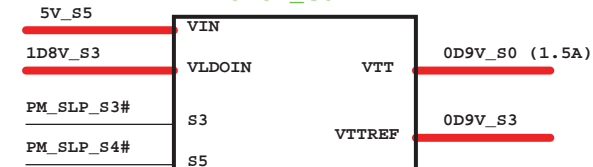
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MAX8770



MAX8717
1D8V/1D05V

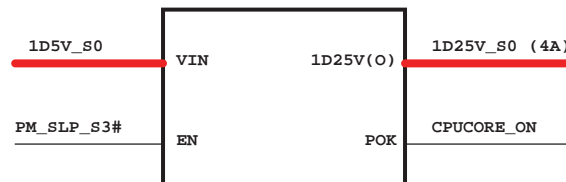


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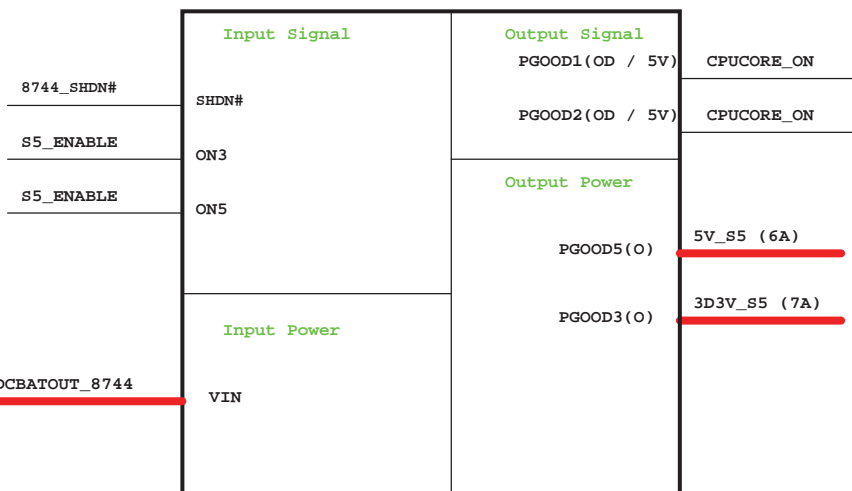
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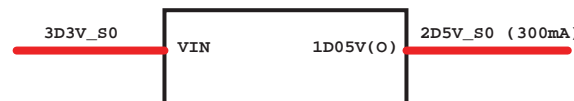


APL5915

MAX8744
5V/3D3V

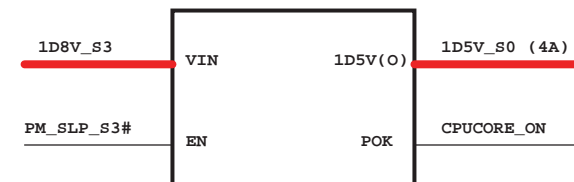


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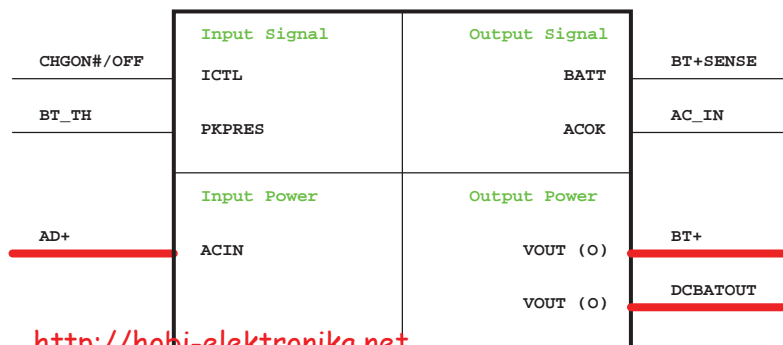
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APL5912

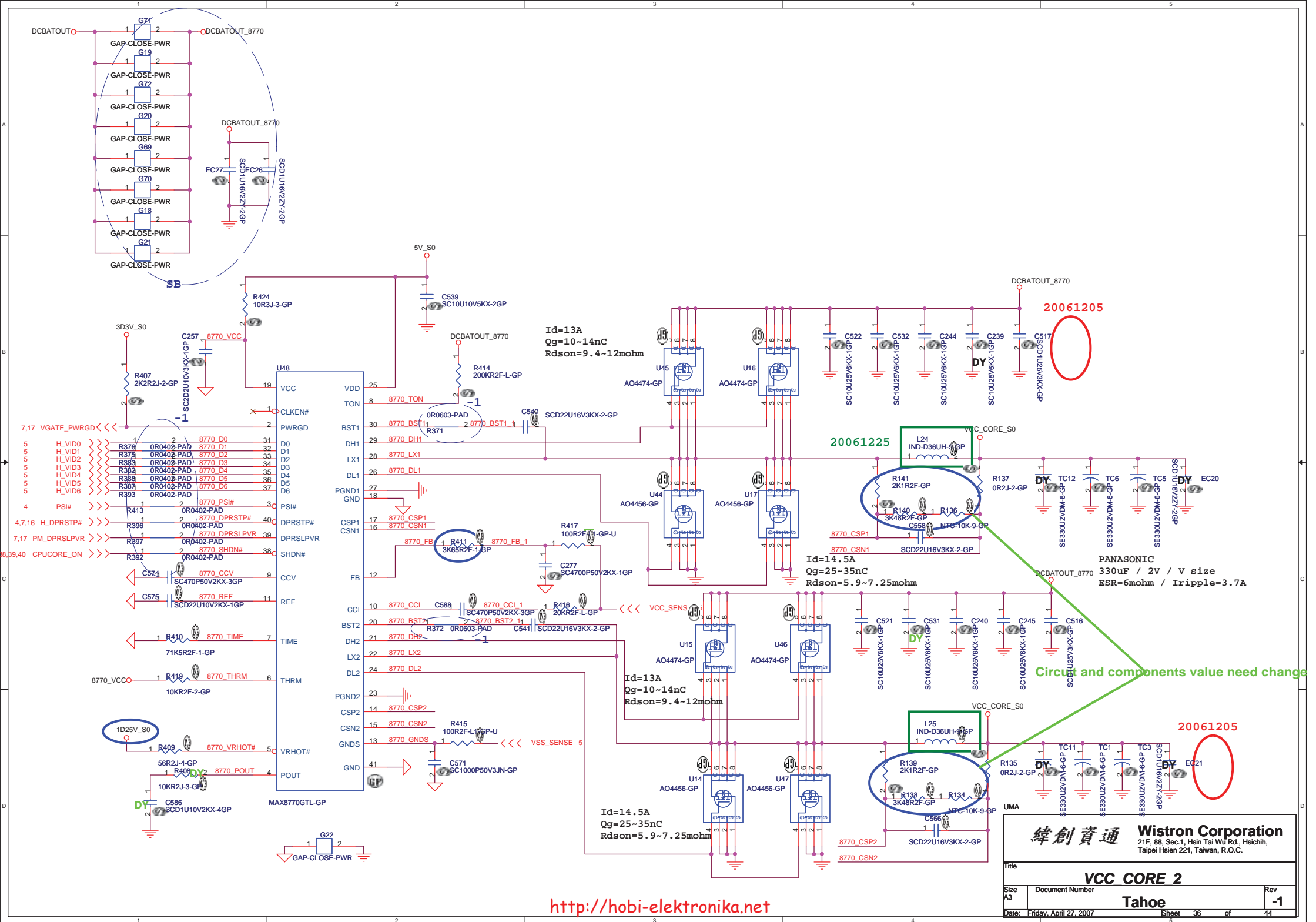
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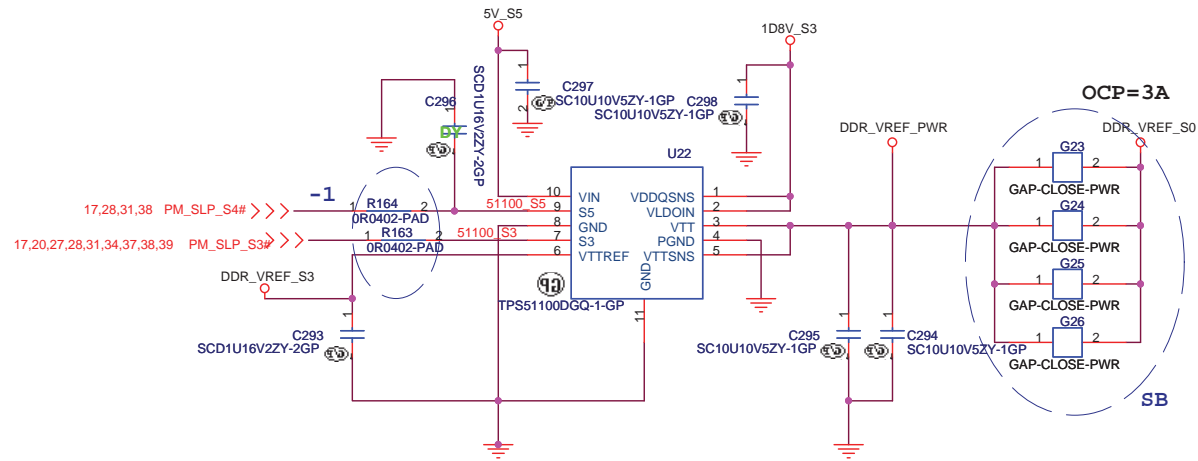
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緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Power Block Diagram	
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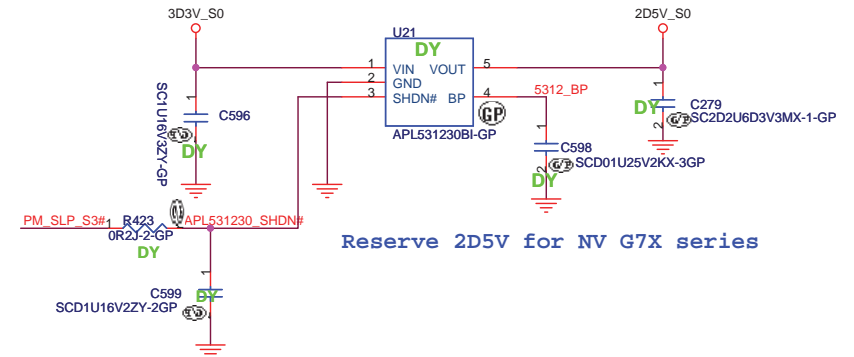
Tahoe



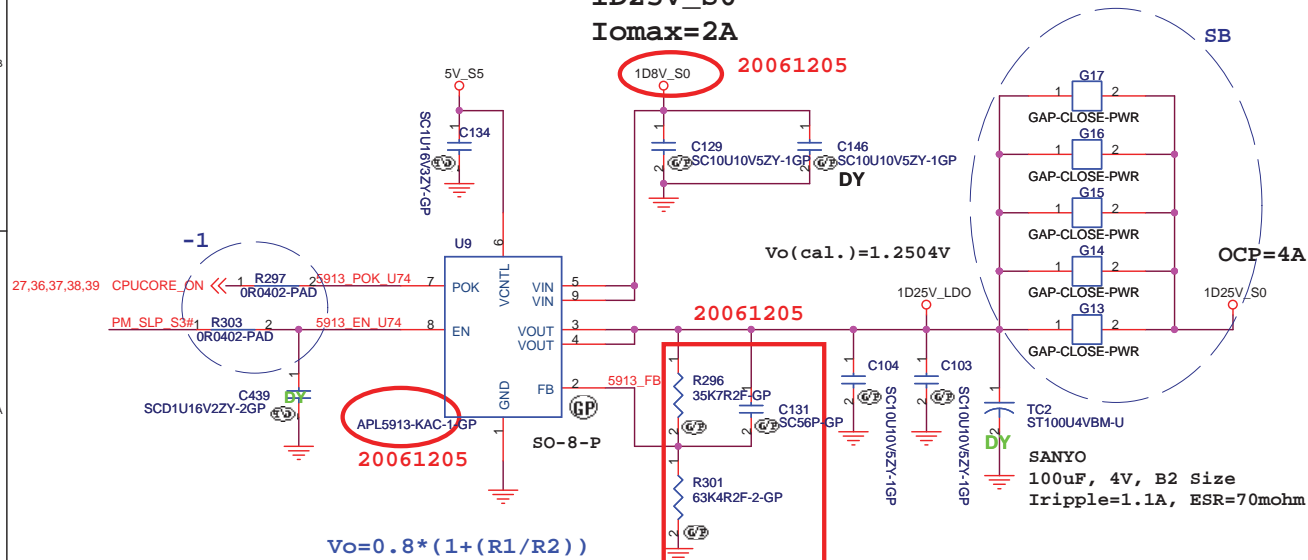
0D9V_S3
Iomax=0.5A



2D5V
I_{omax}=130mA



1D25V_S0
Iomax=2A



UMA

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title	1D25V/2D5V//1D05V/0D9V
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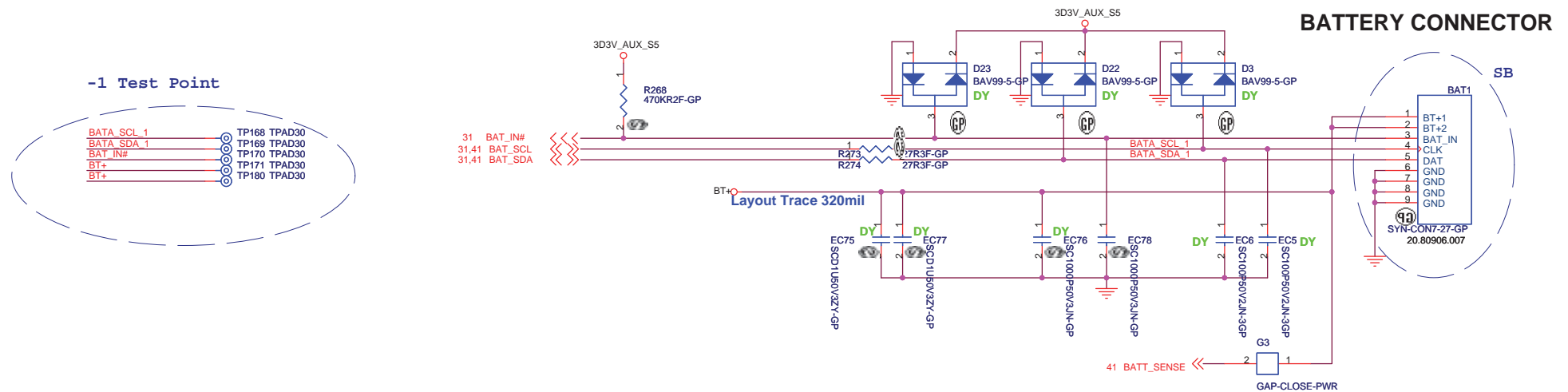
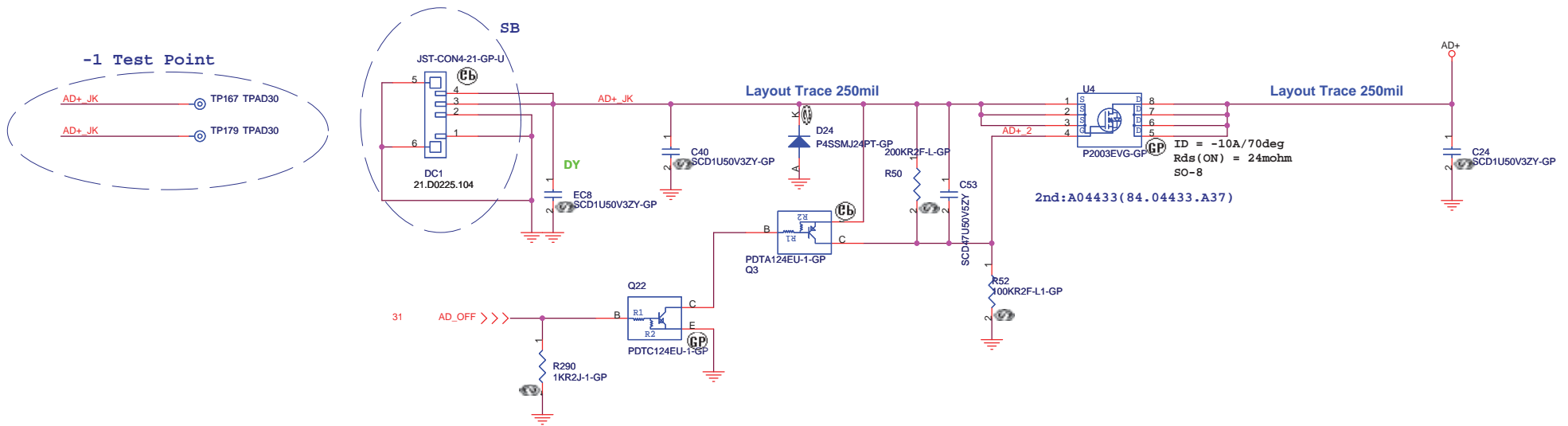
Tahoe

Rev
-1

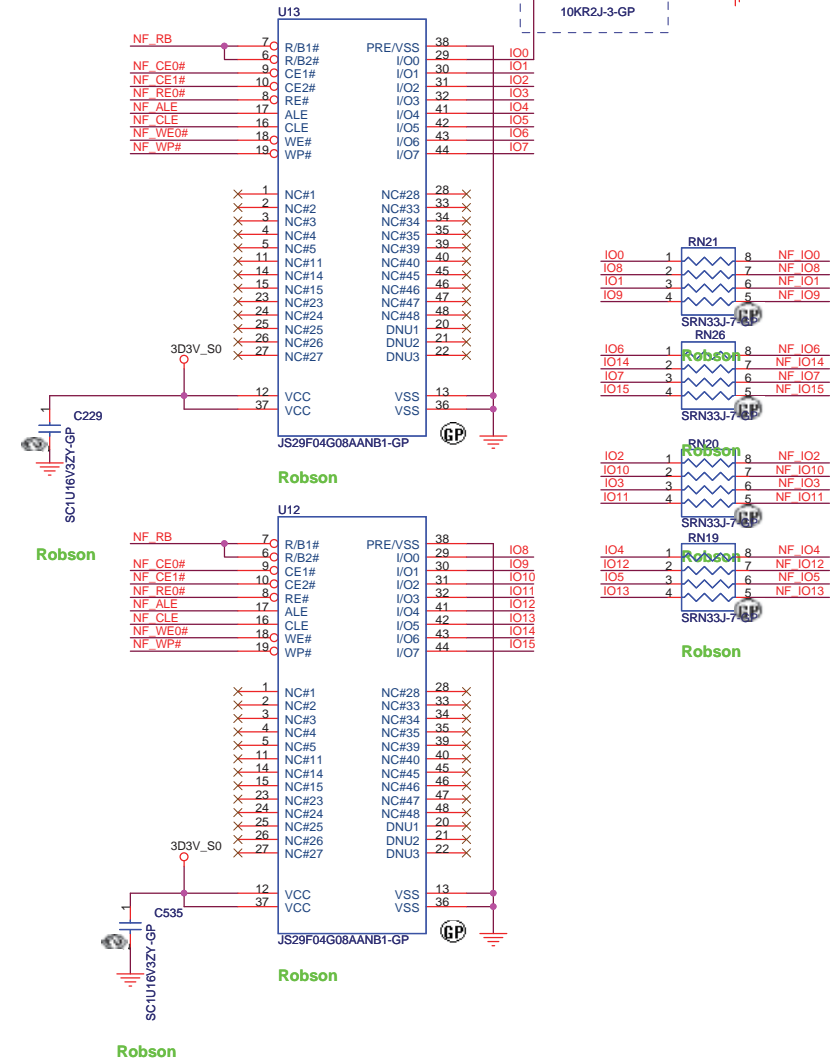
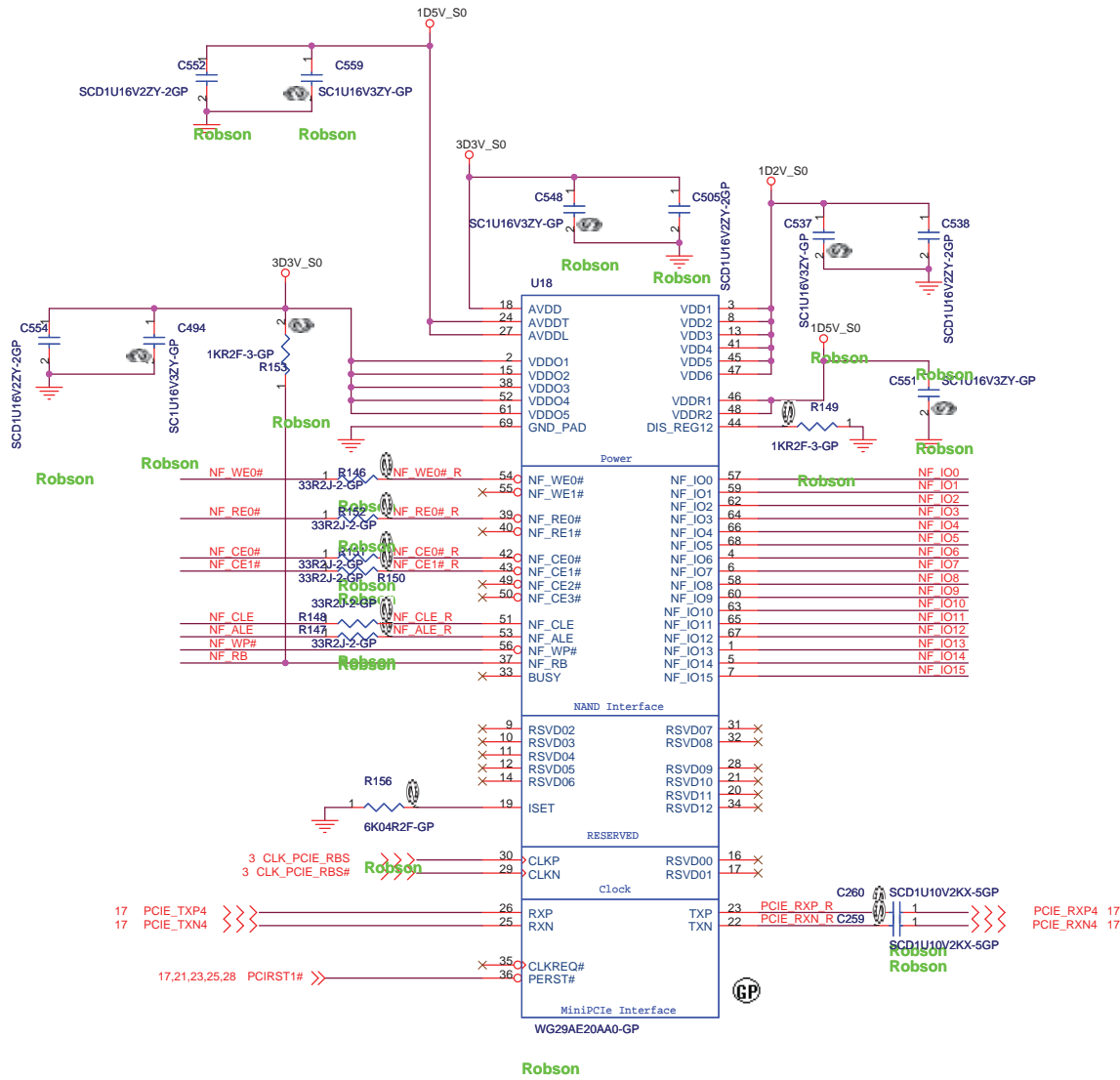
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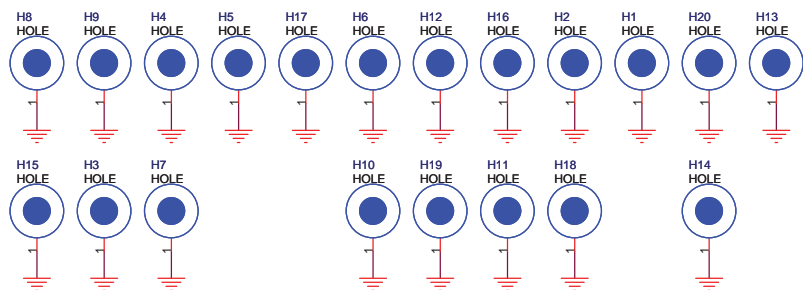
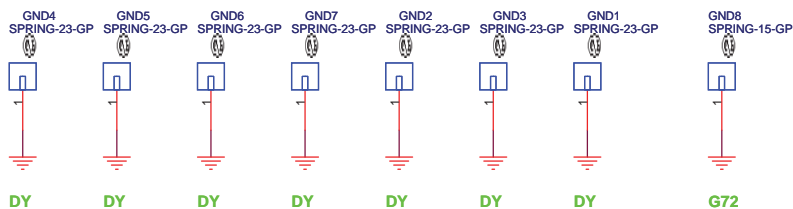
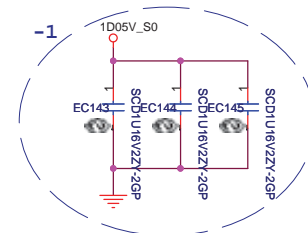
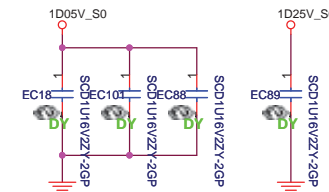
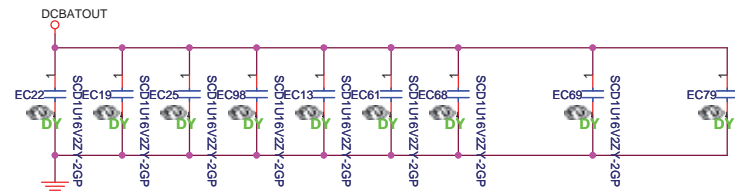
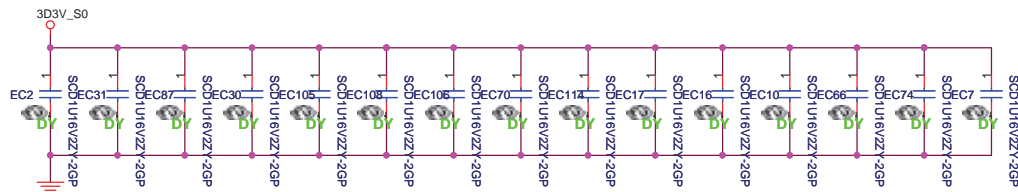
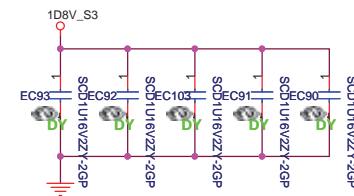
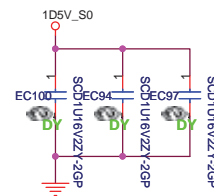
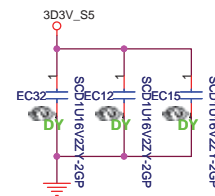
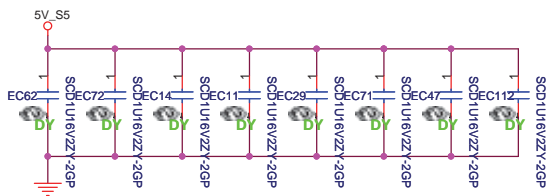
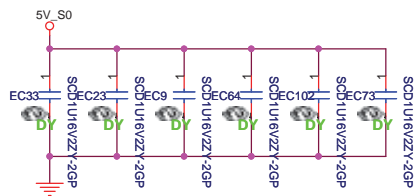
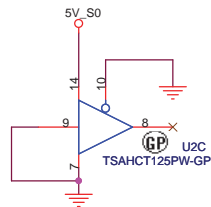
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Adaptor in to generate DCBATOUT



R632
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DESTUFF: INDICATES A 4KB VIRTUAL PAGE





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Title		Wistron Corporation	
Size		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Document Number		EMI/Spring/Boss	
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